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A HIGH-RATE DIGITAL DATA RECORDING APPLICATION OF THE BELL AND --ETC(U)
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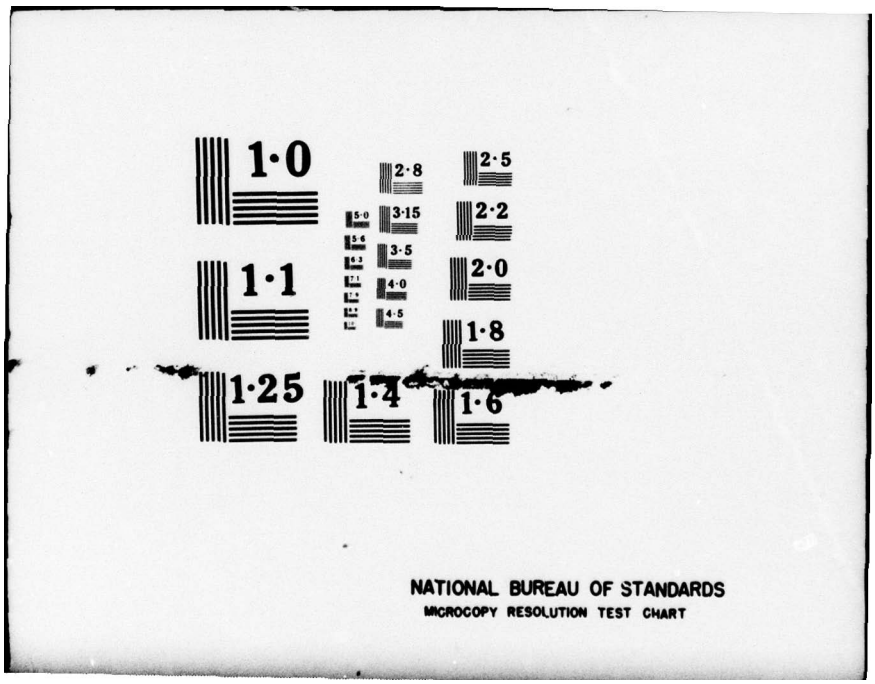
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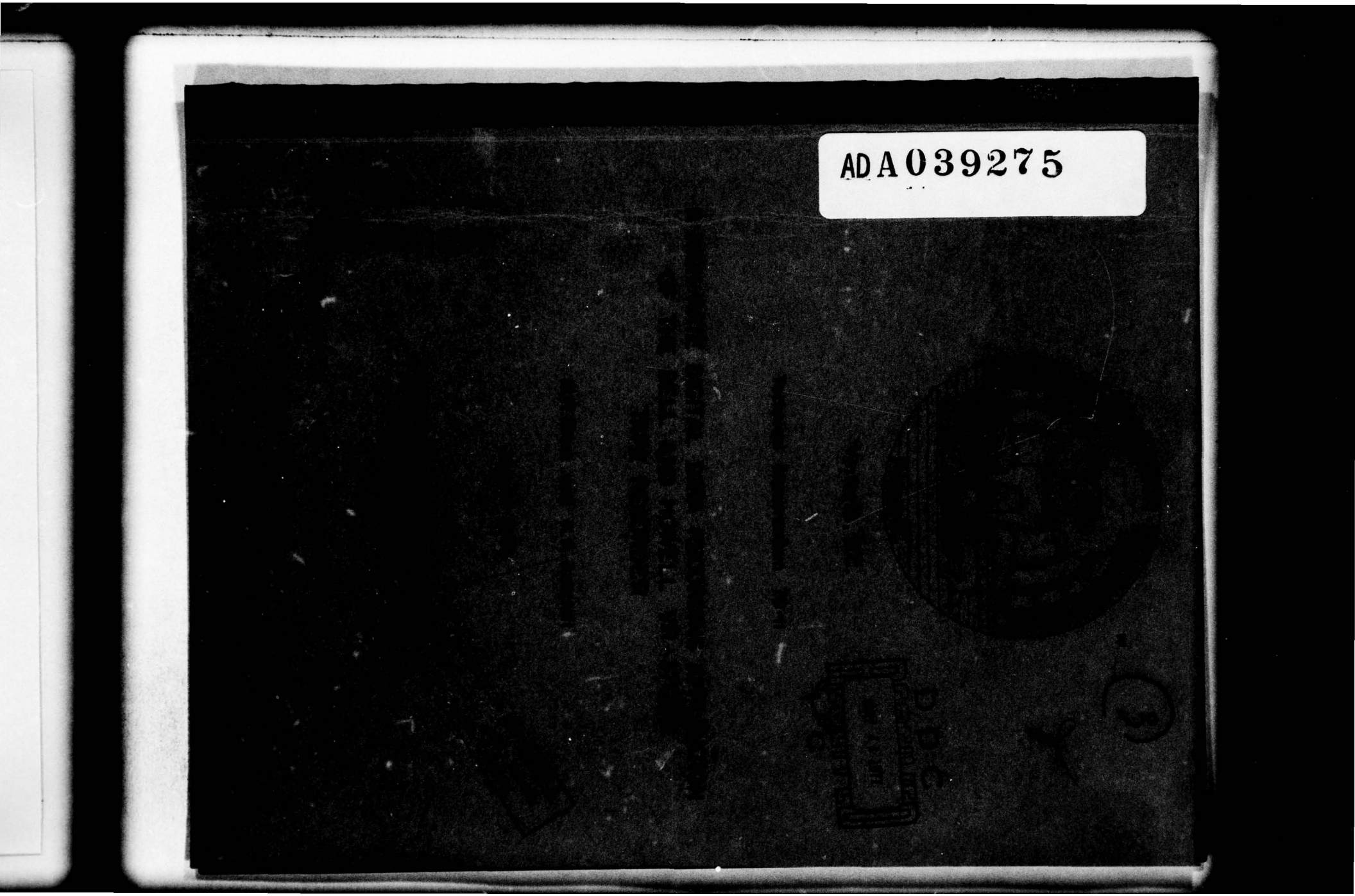

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(6) A HIGH-RATE DIGITAL DATA RECORDING APPLICATION OF THE BELL AND HOWELL VR-3700B TAPE RECORDER

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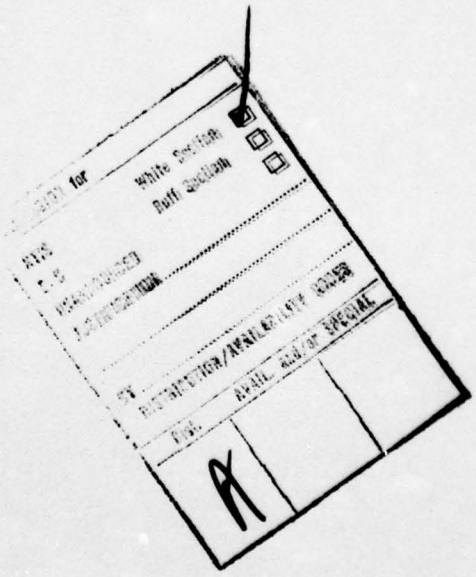
ABSTRACT

A tape recording system was assembled to record scientific data on board a research vessel. Digital data equivalent to a single serial bit stream with a clock rate of 10.6 mHz were multiplexed onto six serial pulse-code-modulation channels of a Bell and Howell VR-3700B high-density digital tape recording system. The Bell and Howell enhanced-non-return-to-zero (ENRZ) code was used with a tape speed of 120 inches per second and a packing density of 16,500 bits per inch. Auxiliary data including compass reading, time, ship's speed, event count, trial number, and analog amplifier gain were recorded on a seventh digital channel of the tape recorder. An interface system between the data source and the tape recorder was developed for handling and formatting both recorded and reproduced data. Buffer memory arrays made up from the Fairchild Semiconductor 9403 first-in first-out LSI memory circuits were used to distribute the data to the six channels of the tape recorder and to deskew and restore the reproduced data to their original format. Facility was provided to allow playback of recorded data at one thirty-second times real time for detailed analysis. Overall error rate for reproduced data was about one error per one million data bits. Error rate was found to be almost entirely tape dependent as some recorded tapes could be reproduced with zero errors.



LIST OF MNEMONICS USED

BCD	Binary Coded Decimal
CPSI	Serial Input Clock Pulse
CPSO	Serial Output Clock Pulse
DS	Serial Data Input
ENRZ	Enhanced Non- Return to Zero
FIFO	First-In First-Out
FM	Frequency Modulated
I/O	Input-Output
IRIG	Inter-Range Instrumentation Group
LED	Light-Emitting Diode
LS	Low-power Schottky clamped
LSI	Large Scale Integration
MR	Master Reset
PCM	Pulse Code Modulation
PL	Parallel Load Clock Pulse
TOP	Transfer Output Parallel Clock Pulse
TTL	Transistor-Transistor Logic

This report describes a high-rate, large-volume data recording system which was developed by the authors at the Defence Research Establishment Pacific in 1975. The recording system was used on board ship and in the laboratory. The data consisted of sets of ninety-six 8-bit parallel-digital words. Clock rate for these data words was 2.65 MHz.

The goals of the data recording assignment were as follows:

1. To record one half of the data, that is 48 adjacent words for periods up to 12 minutes.

2. To record auxiliary information associated with the equipment trial series including stop-watch time from a designated trial time zero, ship's compass readings, ship's speed, event count from trial time zero, trial number, analog variable-gain-amplifier control signal and IRIG time-code-B clock signal.

3. To reproduce the recorded data in real time for recorded-data quality monitoring.

4. To reproduce the recorded data at one thirty-second times real time for processing by a programmable digital filter and minicomputer. The purpose of this step in the data analysis process was to reduce the amount of data so that they could be stored on standard computer-compatible tapes. These tapes were used to supply data for analysis using a large computer processor.

A high-density digital pulse-code-modulation (PCM) tape recording system was selected to fulfill this data-recording requirement. The tape transport selected was the Bell and Howell VR-3700B with 1-inch, 14-track, wide-band tape heads. The digital recording mode selected was the Bell and Howell enhanced-non-return-zero (ENRZ) PCM code. Seven channels of ENRZ record and reproduce electronics were used to record the digital data. Specifications for the tape recorder system are given in Appendix I.

Six digital channels were used to record the high-rate data, the additional digital channel was used to record the lower-rate digital auxiliary data, and two channels with analog frequency-modulated (FM) electronics were used to record the variable-gain-amplifier control signal and the IRIG time-code-B signal.

The systems for recording and reproducing the high-rate data and for recording and reproducing the auxiliary digital data are discussed separately.

THE HIGH-RATE DATA RECORDING SYSTEM

The data consisted of 8-bit digital words with a clock rate of 2.65 MHz. One half of these data were to be recorded; so this amount of data is equivalent to a single serial data channel with a data bit rate of 10.6 mHz (8x2.65 MHzx½). This serial data rate is beyond the

The FIFO memory arrays consisted of eight Fairchild 9403 LSI integrated circuits configured two wide and four deep. This gave a memory capacity of sixty-one 8-bit words of 488 bits. For this sytem fifty-three 8-bit words or 424 bits were loaded into each memory in parallel mode and unloaded in serial mode each memory cycle.

The propagation delay of a data word falling through a memory array from input to output was about 1.8μsec; so the start of the serial unload clock pulses (CPSO) had to be delayed by more than 1.8μsec from the first parallel load (PL) pulse as shown in Figure 5.

The six serial data streams from the six record FIFO memory arrays were pased via 50-ohm data buffers to the inputs of the serial-PCM record electronics of the Bell and Howell VR-3700B tape recorder. The 1.9872-MHz serial clock was also distributed to the clock inputs of each of the six channels of the tape recorder. Channels 3,5,7,9,11 and 13 of the tape recorder were used to keep all the high-rate data on one tape head. This was done to minimize reproduce timing problems due to dynamic tape skew and tape stretching between reproduce heads.

THE REPRODUCE DEMULTIPLEX SYSTEM

For the following discussion reference is made to the reproduce timing diagram (Figure 6), the reproduce FIFO memory array diagram (Figure 7), the reproduce timing circuit block diagram (Figure 8) and the clock board block diagram (Figure 9).

The purpose of the reproduce demultiplex system was to reconstitute the data recorded into their original format.

The reproduce FIFO memory arrays were made up of eight Fairchild 9403 LSI integrated circuits configured two wide and four deep similar to the record arrays. The reproduced data and clock signals from each of the six serial PCM reproduce tape channels were connected to the serial data (DS) and serial clock (CPSI) inputs of each of six reproduce FIFO memory arrays. The serial data from each channel were also clocked into each of six bit-pattern recognition circuits configured to recognize the sync-word pattern used. Upon recognition of the sync word pattern on a particular channel, a sync recognition pulse was generated which was connected to the memory reset (MR) input of the FIFO memory array for that channel. This pulse cleared out the memory and ensured that the first eight bits of the data block, which immediately followed the sync word, would be the first word that appeared at the output of the memory, following reset. The FIFO memory integrated circuits have tri-state outputs; so an 8-bit parallel-data bus was formed by connecting the parallel outputs of the six arrays in parallel.

The reproduced clock signal from tape channel 9 (system channel 4) was connected to the clock board, where a four-thirds frequency conversion was performed by a phase-locked loop (PLL) circuit. This provided 2.65 MHz (1.9872 MHz x 4/3) for the parallel output data clock for real-time reproduce operation, or 82.812 kHz (2.65MHz x 1/32) for the one-thirty-second times real-time reproduce mode. The parallel output data clock was passed from the clock board to the reproduce timing board, where it was

gated to each of the six reproduce memory arrays in sequence. These signals are called transfer output parallel (TOP). The serial clock signal from tape reproduce channel 9 and the sync recognition signal from reproduce system channel 4 were connected to the reproduce timing board to generate the TOP clock gating signal. Output-enable gating pulses were also generated to operate the tri-state outputs driving the parallel data bus. The word zero marker pulse was also regenerated from the sync recognition signal from system channel 4. A track in the middle of the tape, channel 9, was selected to control all the output data timing because it was felt that the reproduce timing errors between tracks were a function of the separation of the tracks on tape. The most critical time in the reproduce system is shown in Figures 10 and 11. This was the time between the end of the TOP pulses controlled by the clock on tape channel 9 and the sync recognition pulse of another tape channel which was controlled by the clock and data of that channel. Dynamic tape skew caused variations in this time. As shown in Figure 11, about 2.5 μsec was provided as a guard zone to permit these variations to occur without interfering with the operation of the system. The maximum variation observed in this guard zone was about ± 1 μsec between system channels 1 and 4.

The demultiplexed data consisted of 48 of the original 96 parallel 8-bit data words with data word clock and word zero marker pulse.

THE DATA INPUT SYSTEM

For the following discussion of the data input system, reference is made to the system block diagram (Figure 1) and the interface system block diagram (Figure 12).

Data and clock signals and the word zero reference signals were coupled to the data recording system via differential line drivers, each driving fifty feet of twisted-pair cable. The signals were received on differential line receivers and passed on to the recording system.

A simulated data source and clock were made available by switch selection for test purposes. The simulated data consisted of the output of a 0-to-95 counter which was reset by the word zero pulse. With this counter coupled into the system, each word in the data block was stationary and identifiable. By switch selection it was possible to operate this counter from the data source clock and word zero signal or from clock and frame marker signals generated from an internal clock.

Demultiplexed data, clock and word zero marker signals were coupled to the data source for monitoring via differential line drivers, each driving fifty feet of twisted-pair cable. The signals were received by differential line receivers and were coupled to the data source via logic buffers.

THE TEST-CHANNEL SYSTEM

As shown in the system block diagram (Figure 1), a single test channel was incorporated into the system for the purpose of providing a known signal which was passed through the formatting, recording and

reproduce system and monitored for signal quality. A known analog signal was passed to an analog-to-digital converter. The eight-bit-parallel-digital output of the converter was inserted into the input parallel data stream in place of one of the data words selected by a front-panel, two-digit, thumb-wheel switch. A bank of eight digital-to-analog converters were coupled to the test-channel recording system so that each converter could select one of the 48 data words being recorded and provide analog output of the digital data. Channel selection was made by a two-digit, thumb-wheel switch on the front of each converter. The designated test channel was selected and displayed on an oscilloscope to monitor total system operation from data input to data output. A real-time spectrum analyser and three dimensional display were used in conjunction with one of the digital-to-analog converters to observe the data from a single source in the frequency domain.

THE SYSTEM PHYSICAL CONFIGURATION

The record and reproduce interface system was constructed on wire-wrappable boards manufactured by Digital Equipment Corporation. The record timing board is shown in Figure 13. The 24-pin Fairchild 9403 FIFO memory integrated circuits were mounted on separate printed circuit boards which were attached to the wire-wrappable boards. A record FIFO memory array board for a single channel is shown in Figure 14 and a reproduce FIFO memory array for a single channel is shown in Figures 15 and 16. The reproduce array board also contains the sync word recognition logic for a single channel.

Power supply current requirement for each record memory board was 1.1 amps and for each reproduce memory board was 1.34 amps. Initially significant voltage drops occurred along the power-supply connections; so copper-strip bus lines were added to the board connector back plane, extra connector pins were used for each board, and heavier power-supply bus lines were added onto each board. Separate five-volt power supplies were used for the record memory boards, the reproduce memory boards, and the other TTL logic circuits so that each could be adjusted independently of the others.

The front panel of the system is shown in Figure 17 with the access door closed, and is shown in Figure 18 with the access door open. The serial data signals to each tape-recorder record channel and from each reproduce channel, and the sync word recognition pulses from each channel were made available on the front panel. Alarm lights were provided to indicate loss of sync word recognition on each channel.

The test-channel selector switch, test-channel on-off switch, sector select switch, and bypass-run switch are shown in Figure 17. The bypass-run switch allowed the tape recorder to be bypassed. This feature proved most useful for system testing without having to pass tape through the tape recorder.

THE AUXILIARY DATA CHANNEL SYSTEM

For the following discussion reference is made to the auxiliary data channel system block diagram (Figure 19).

The auxiliary data channel system took data from seven sources and formed the data into an 8-word PCM frame of 16-bit words. This serial bit stream was recorded via a single PCM channel of the tape recorder with a serial bit rate of 1 MHz. The frame format is given in Table 1. The first word in the frame is the frame sync word.

The second and third words represent time from milliseconds to minutes in BCD format from trial time zero, designated by operating a front-panel, reset button. Minutes and seconds were displayed on a 4-digit, front-panel display.

The fourth word was a 10-bit digital word indicating ship's heading. These data were coupled to the recording system from the ship's compass system via line drivers, twisted-pair cables and line receivers.

The fifth word was a 4-digit word in BCD format indicating the frequency in Hz of the ship's speed tone generated by a doppler speed log system.

The sixth word was obtained from a 4-digit BCD counter of experimental events. This counter was also coupled to a 4-digit, front-panel display, and was reset with the time zero reset button.

The seventh word was obtained from a 3-digit BCD counter which held the trial number. This counter was also coupled to a 3-digit front-panel display. Trial number was advanced by operating a front-panel push button.

The eighth word was obtained from a 12-bit analog-to-digital converter. The analog variable-gain-amplifier control signal from the data system was coupled to this converter.

The serial-PCM data bit stream was coupled to a single digital channel of the tape recorder, channel 8. Reproduce data and clock were coupled back into the auxiliary data channel system and a tape recorder bypass switch was provided. The sync word was decoded and used to reset a word-position counter. A serial-to-parallel conversion of the data words was performed and the parallel data words were coupled to the input word of microcircuit input-output (I/O) board of a Hewlett-Packard 2100 minicomputer. Specific data words were requested by the I/O board output word according to the format given in Table 2. Flag sets were provided to the I/O board when the data word requested appeared at the input word pin connections. New data were made available every 128 μsec in the real-time reproduce mode and every 4.096 msec in the one-thirty-second times real-time reproduce mode.

A single monitor channel of reproduced data was provided with a 4-digit display, coded for BCD. Data channel selection was by a 7-position switch. This switch also controlled the enable line on a 12-bit digital-to-analog converter which was coupled to the reproduce parallel data lines, and analog output was made available on the front panel.

The auxiliary data channel system was constructed on four Digital Equipment Corporation wire-wrappable boards capable of holding fifty integrated circuits each.

The Numeric displays were mounted on printed circuit cards attached to two of the wire-wrappable boards.

The front panel is shown in Figure 17, and the unit with the card access door open in shown in Figure 18.

SYSTEM DEVELOPMENT PROBLEMS

The most serious problem experienced was with the Fairchild 9403 FIFO memory integrated circuits. These circuits, particularly when connected in the array configuration, seemed to latch up so that data would not fall through from input to output registers. This problem was related to the power-supply voltage supplied to these circuits. This problem was eventually traced to a manufacturing error in the FIFO integrated circuits. As no correct circuits were available, the defective ones were used. A power supply voltage of 5.5 volts had to be used to get the arrays to operate properly,which is out of specification for transistor-transistor logic. Forced-air cooling was provided to the circuit-card enclosure to decrease the possibility of damage due to excessive power dissipation in these circuits.

The Bell and Howell VR-3700B tape system and ENRZ-PCM electronics performed very satisfactorily. Scotch 890 tape was recorded with a bit density of 16,560 bits per inch. Overall data error rate through the reproduce and demultiplex system was about one error per one million data bits. Error rate was found to be almost entirely tape dependent as some recorded tapes could be reproduced with zero errors. Tapes were used directly from stock without being passed through a tape cleaner as one was not available. It was observed that the tape quality improved after a number of passes through the tape machine as this provides some measure of tape cleaning. A precision glass take-up reel was used.

TABLE 1. DATA WORD FORMATS

BIT	WORD1 SYNC	WORD2 TIME MILLISECS	WORD3 TIME SECS-MINUTES	WORD 4 HEADING	WORD5 SHIP'S SPEED HZ	WORD6 EVENT COUNT	WORD7 TRIAL NO.	WORD8 GAIN
15	1	0	0	H9	SSD1000	PD1000	0	G11
14	1	0	40m	H9	SSC1000	PC1000	0	G11
13	1	0	20m	H9	SSB1000	PB1000	0	G11
12	1	0	10m	H9	SSA1000	PA1000	0	G11
11	0	.8	8m	H9	SSD100	PD100	TD100	G11
10	0	.4	4m	H9	SSC100	PC100	TC100	G10
9	0	.2	2m	H9	SSB100	PB100	TB100	G9
8	0	.1	1m	H8	SSA100	PA100	TA100	G8
7	1	.08	0	H7	SSD10	PD10	TD10	G7
6	1	.04	40S	H6	SSC10	PC10	TC10	G6
5	0	.02	20S	H5	SSB10	PB10	TB10	G5
4	0	.01	10S	H4	SSA10	PA10	TA10	G4
3	1	.008	8S	H3	SSD1	PD1	TD1	G3
2	0	.004	4S	H2	SSC1	PC1	TC1	G2
1	1	.002	2S	H1	SSB1	PB1	TB1	G1
0	0	.001	1S	H0	SSA1	PA1	TA1	G0

TABLE 2. OUTPUT WORD REQUEST CODING

I/O CARD OUTPUT WORD	
Other Bits Not Used	
Bits 2 1 0	Word Requested
0 0 1	Time Millseconds
0 1 0	Time Seconds--Minutes
0 1 1	Ship's Heading
1 0 0	Ship's Speed Hz
1 0 1	Event Count
1 1 0	Trial Number
1 1 1	Gain

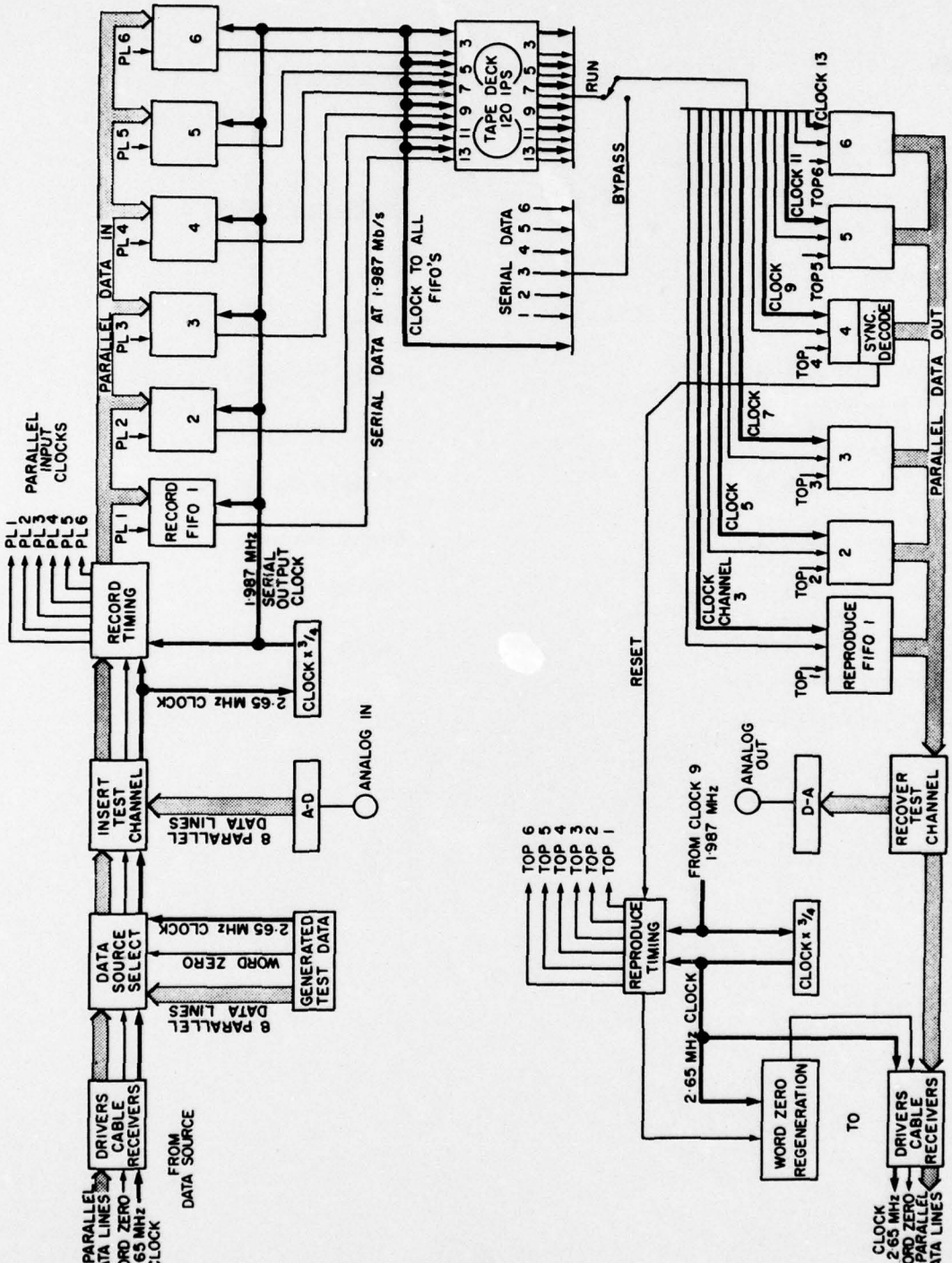


Figure 1: System block diagram.

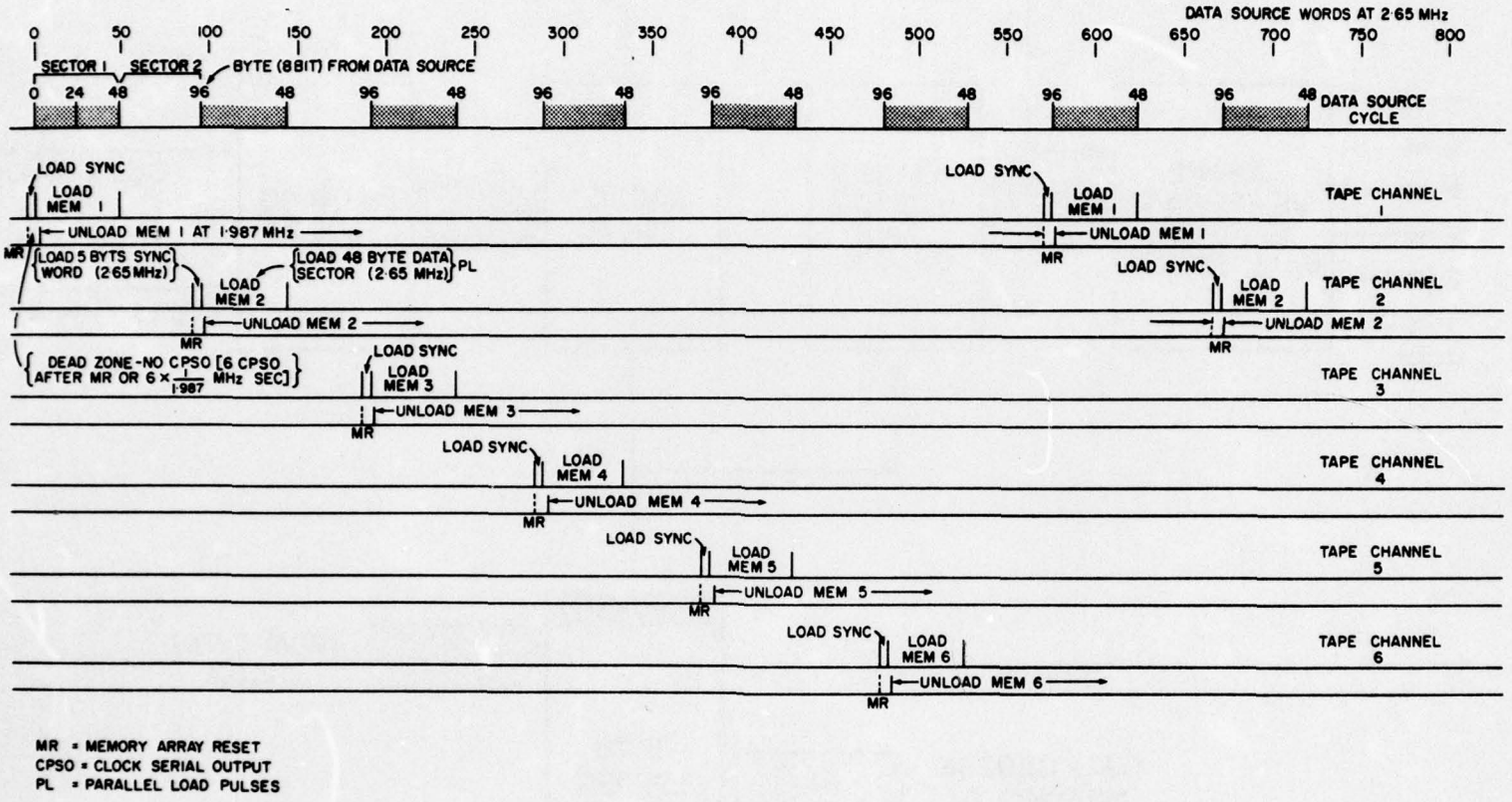


Figure 2: Record timing diagram.

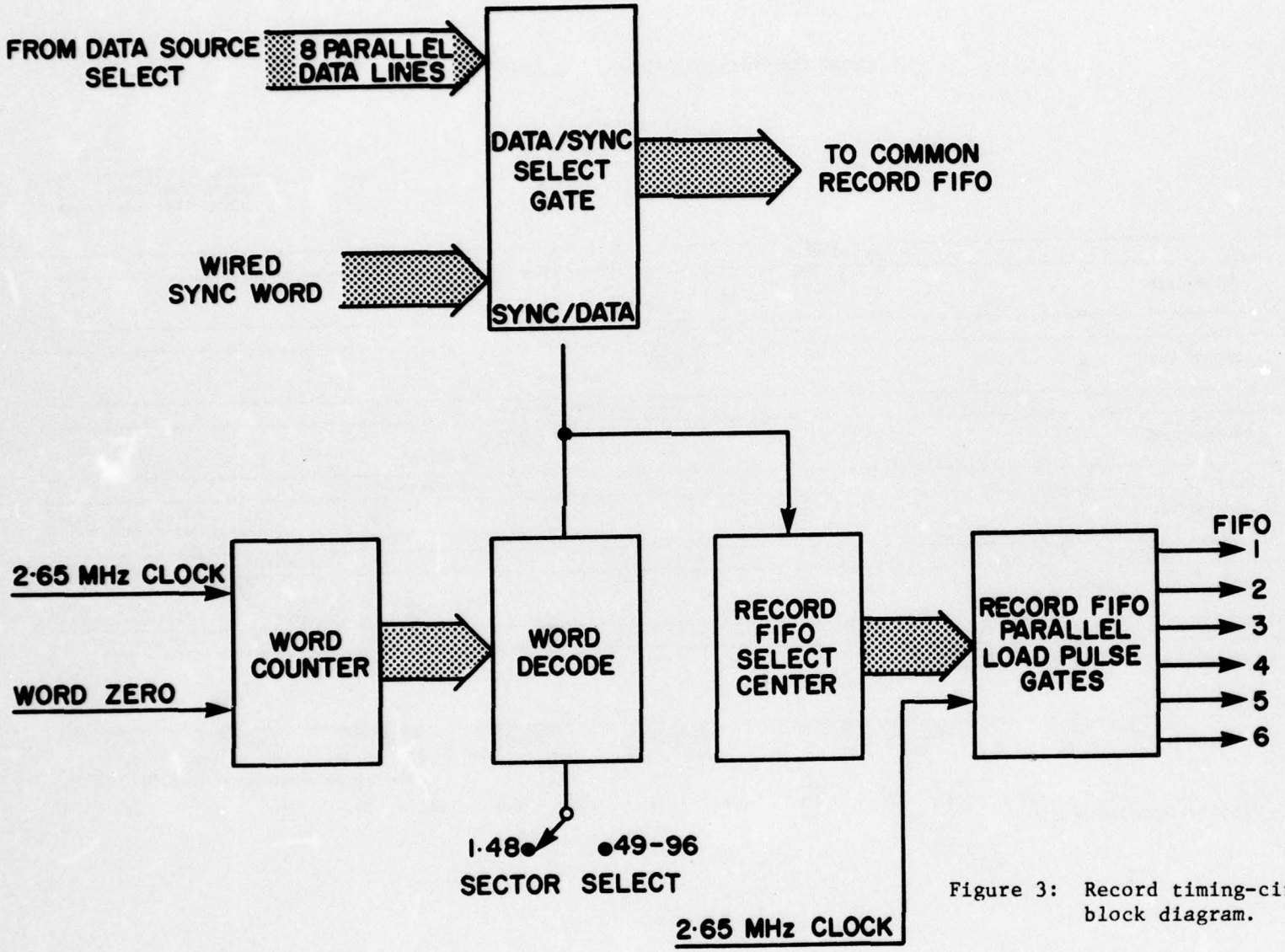


Figure 3: Record timing-circuit block diagram.

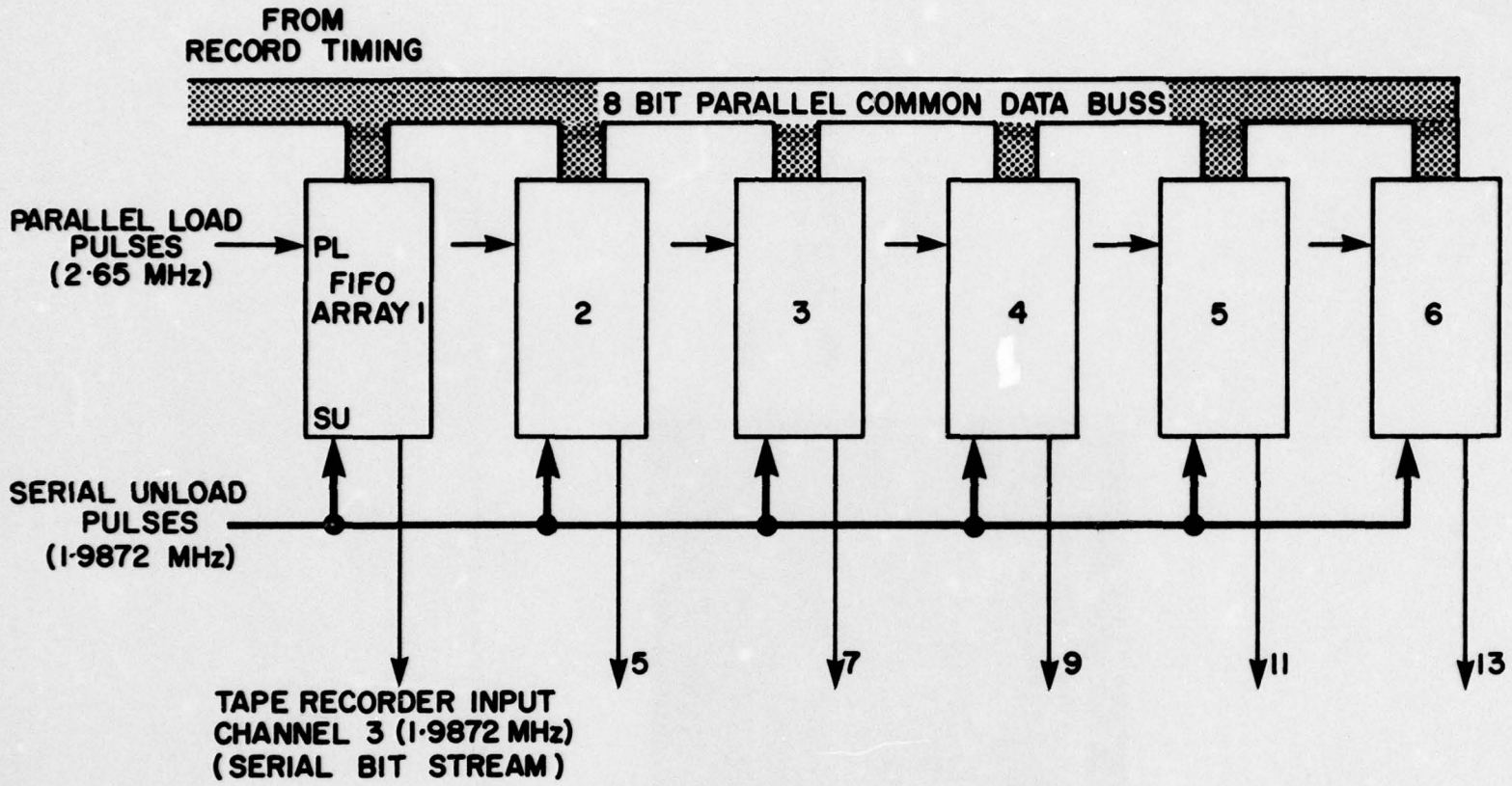


Figure 4: Record FIFO memory array diagram.

NOTE: STAGGERED RECORDER CHANNEL UTILIZING ONE HEAD STACK FOR REDUCED DYNAMIC SKEW

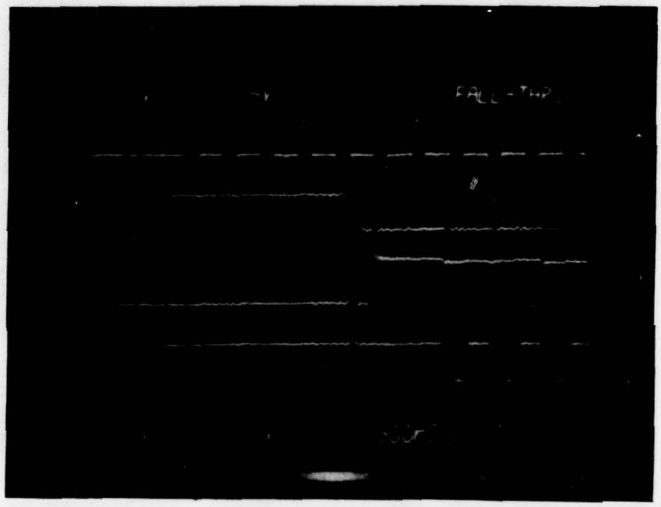


Figure 5: Oscilloscope Display of Record Timing Signals.

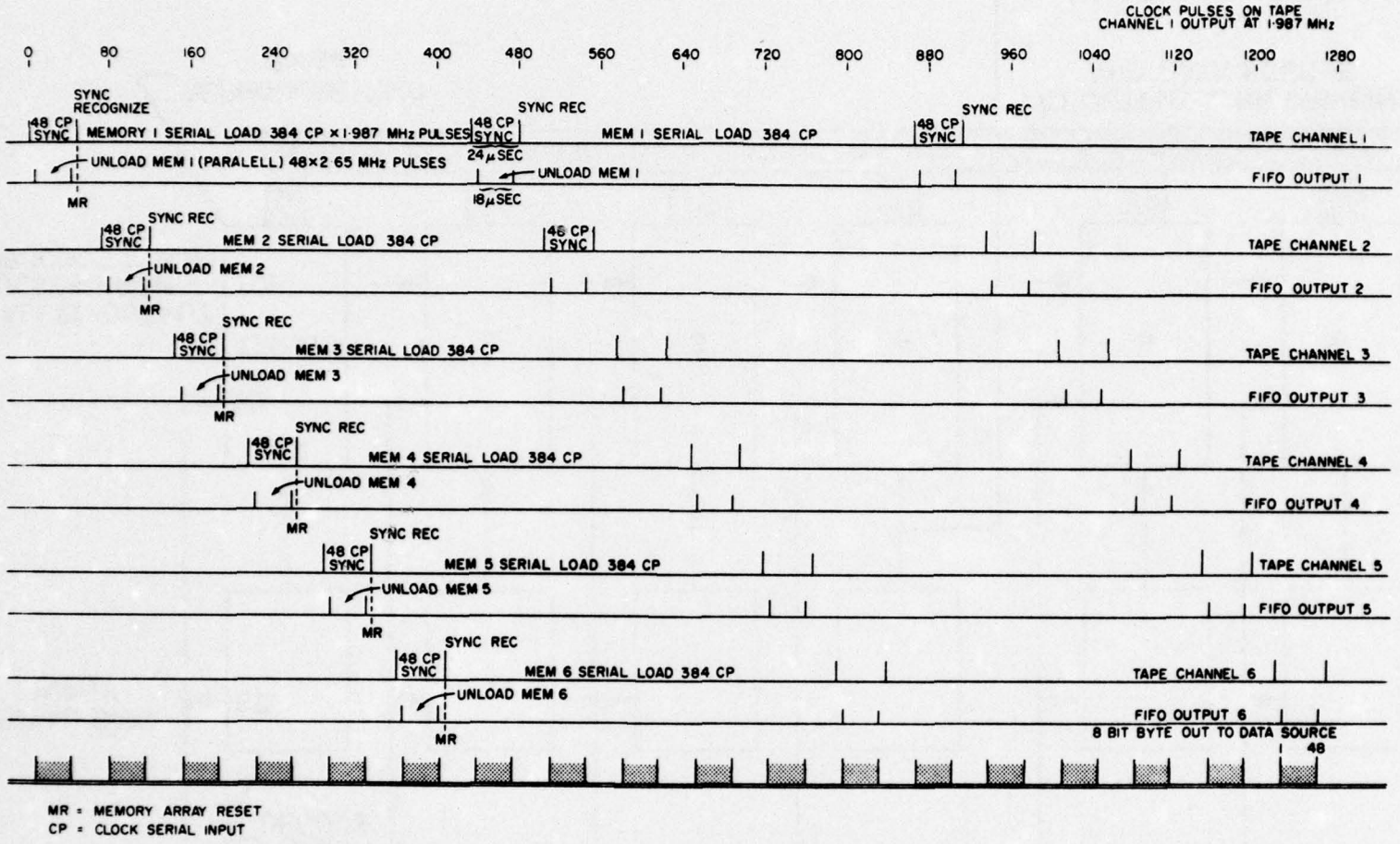


Figure 6: Reproduce timing diagram.

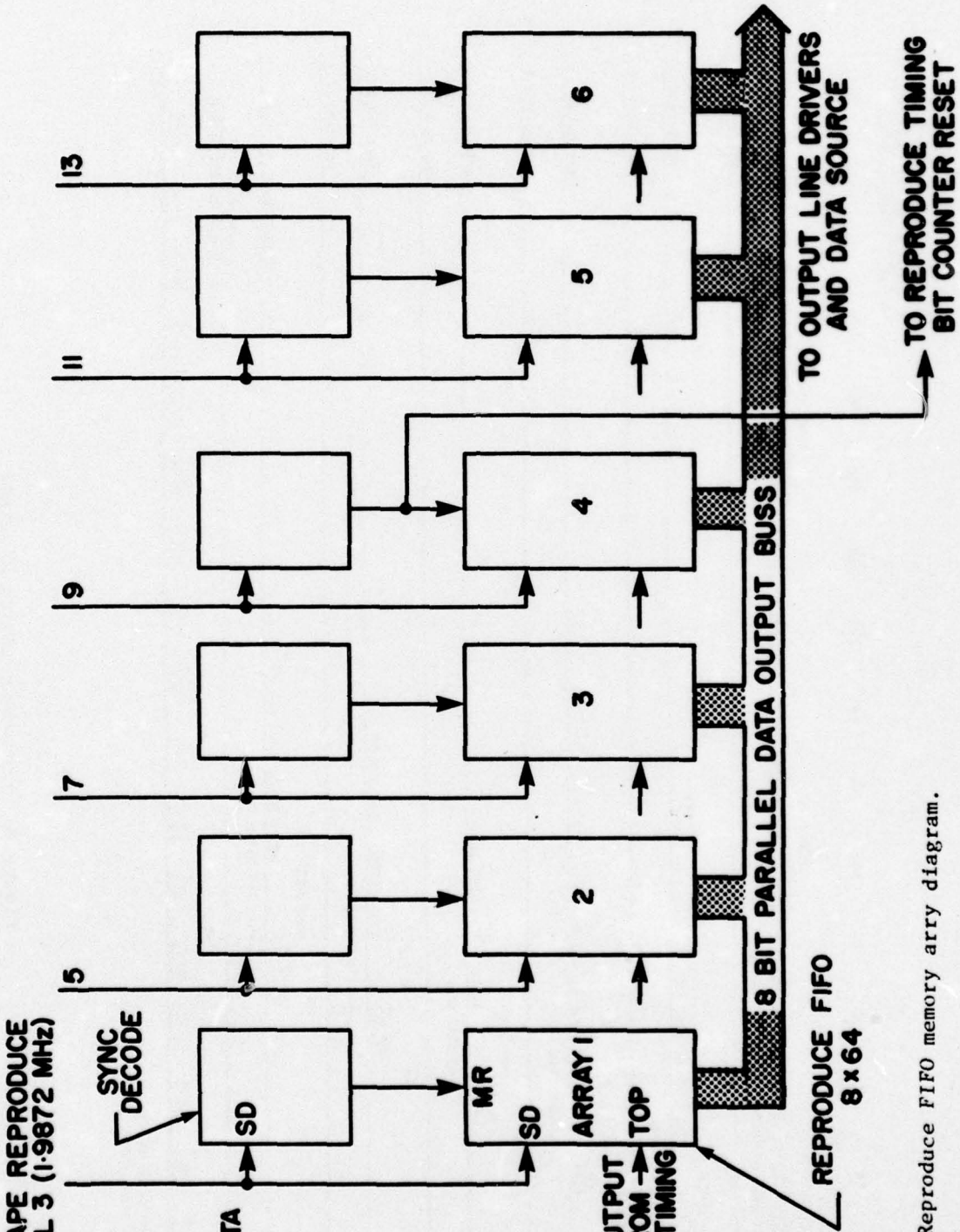
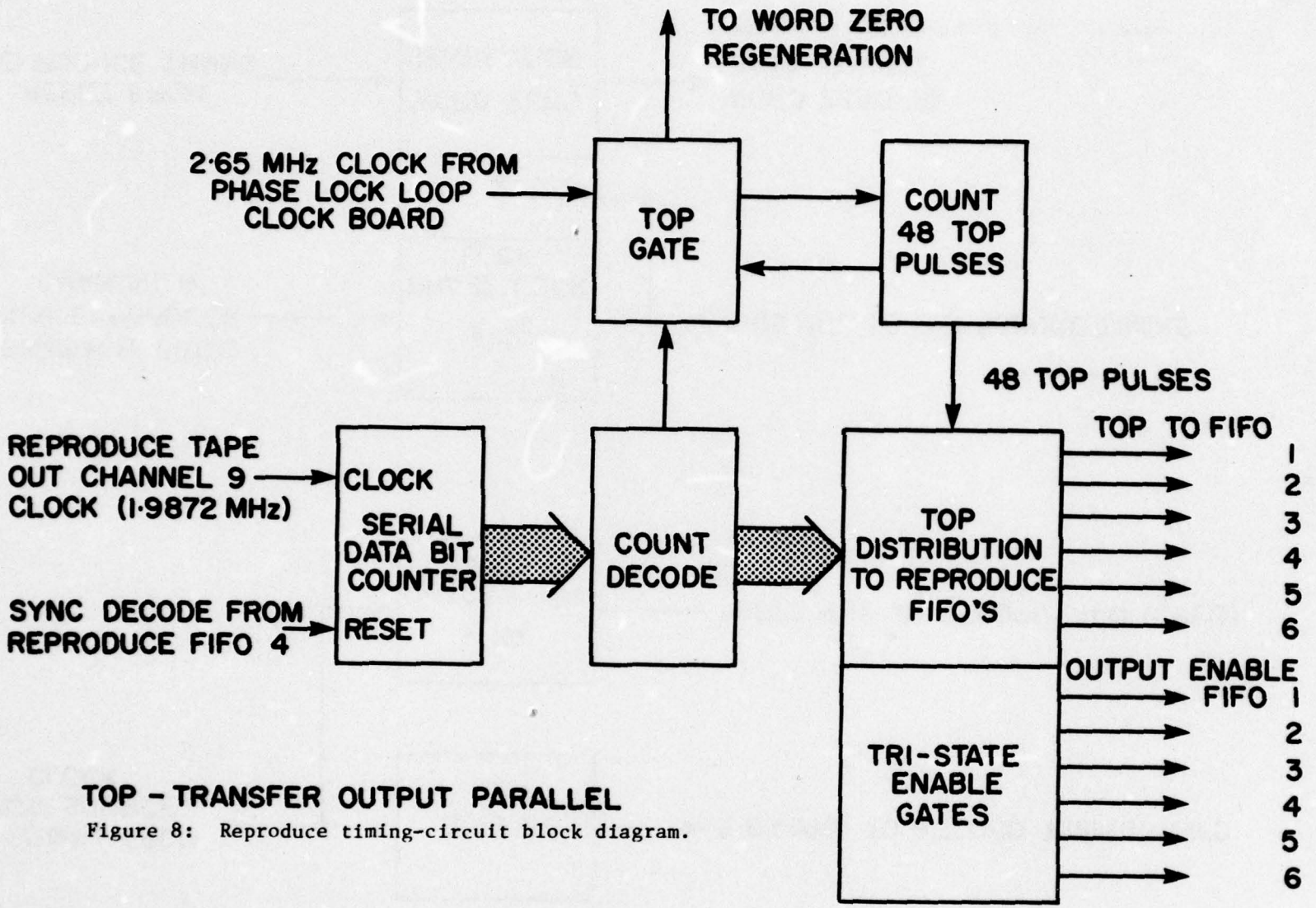


Figure 7: Reproduce FIFO memory arry diagram.



TOP - TRANSFER OUTPUT PARALLEL

Figure 8: Reproduce timing-circuit block diagram.

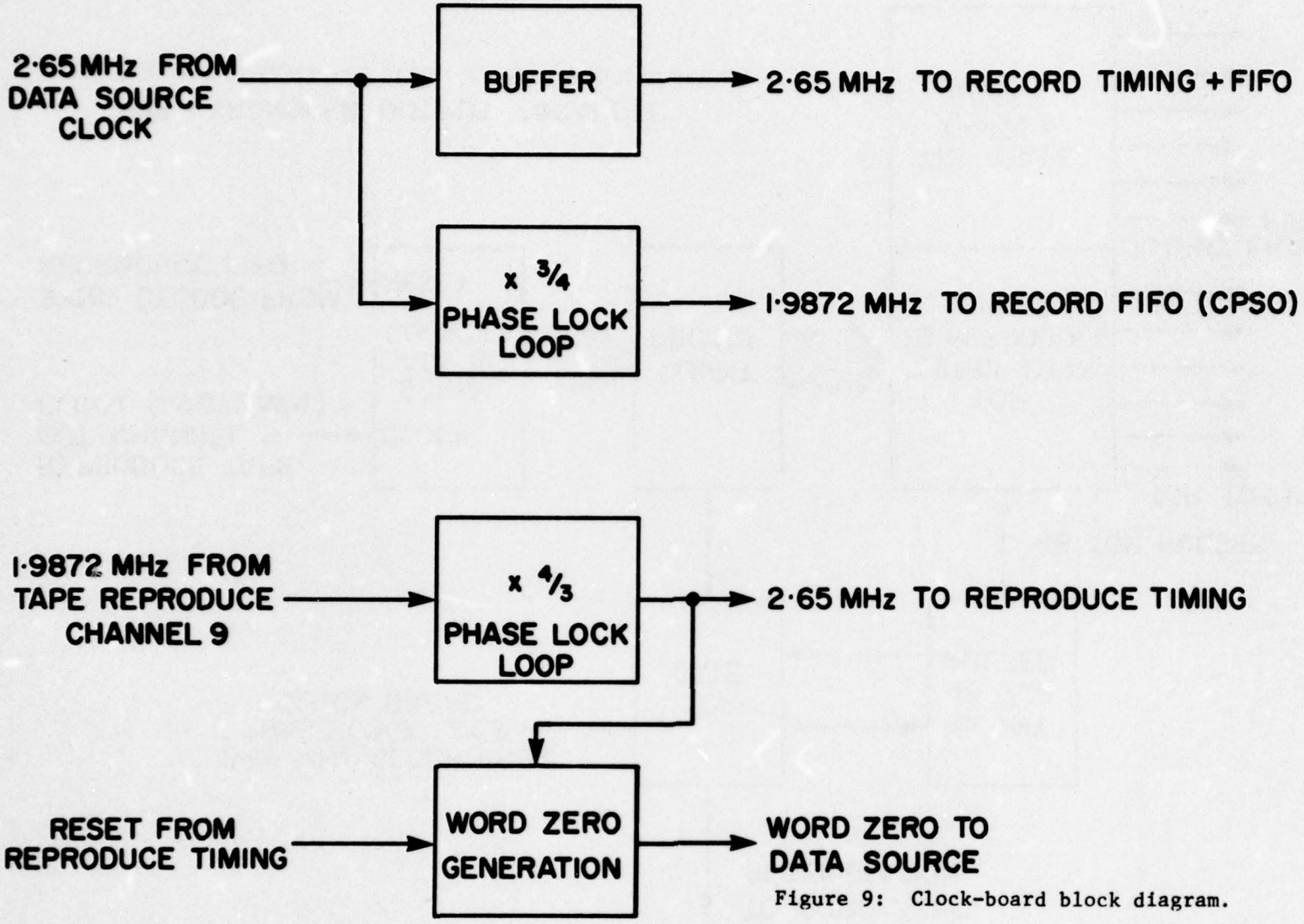
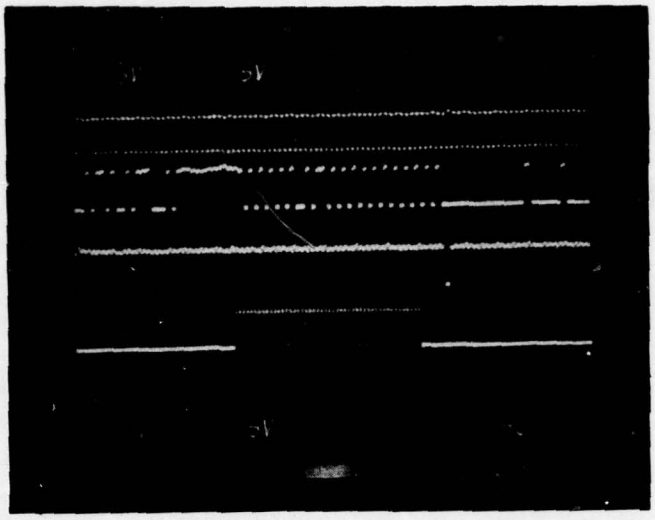
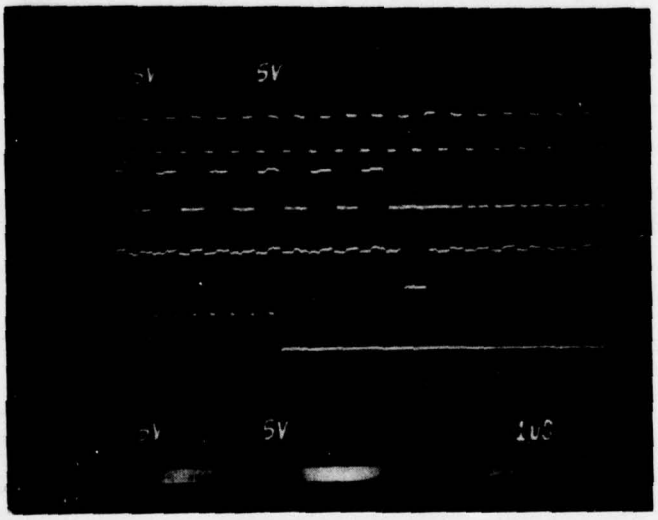


Figure 9: Clock-board block diagram.



- CPSI TO REP.FIFO's
- SERIAL DATA INTO FIFO
- SYNC RECOGNITION PULSE
- TOP PULSES

Figure 10: Oscilloscope Display of Reproduce Timing Signals.



- CPSI TO REP.FIFO
- SERIAL DATA INTO FIFO
- SYNC RECOGNITION PULSE
- TOP PULSES

Figure 11: Expanded Display of Reproduce Timing Signals.

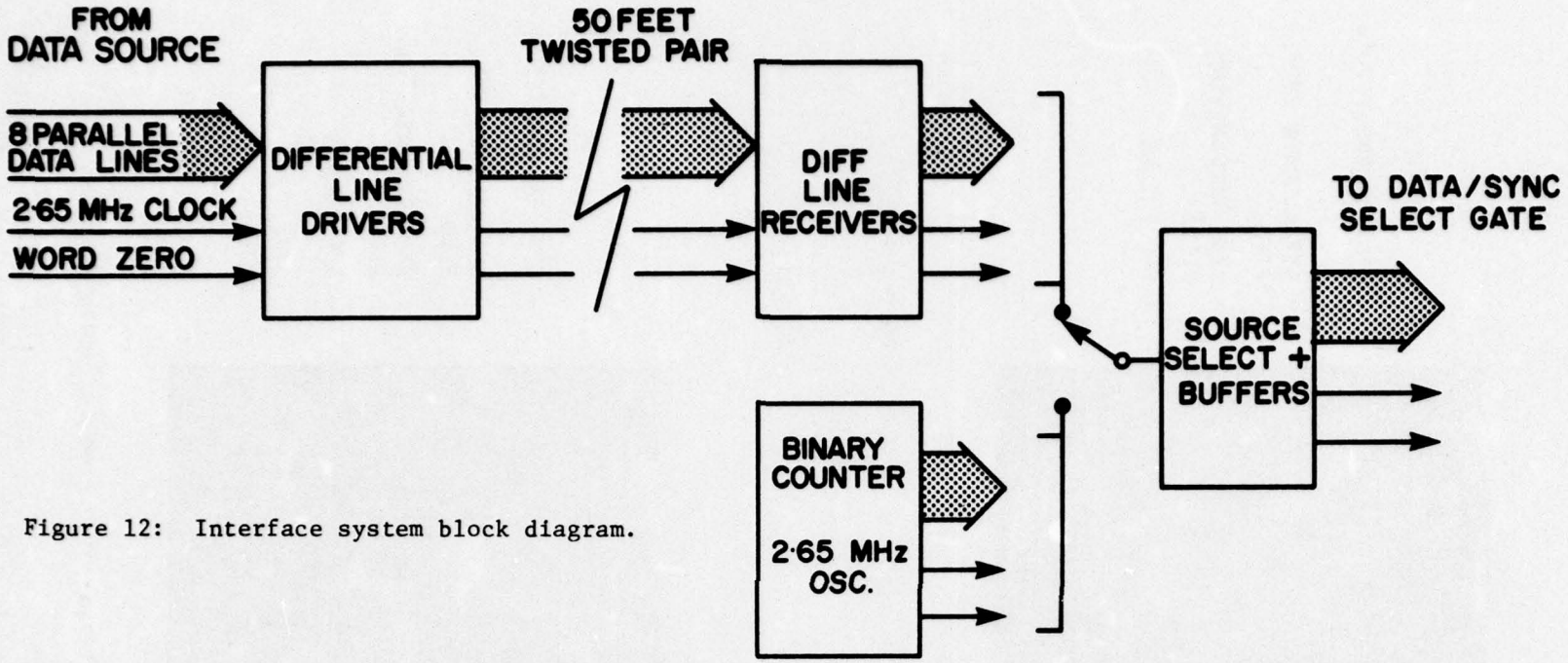
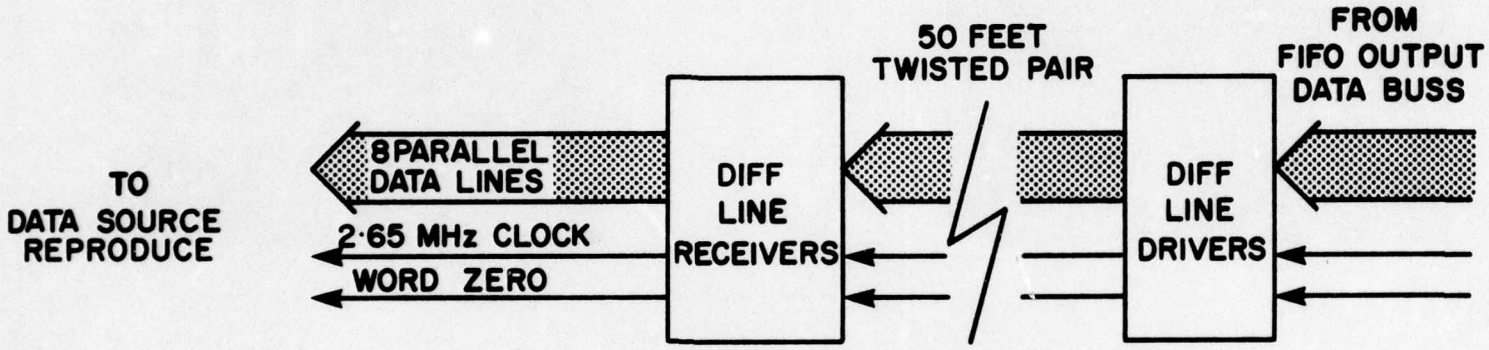


Figure 12: Interface system block diagram.



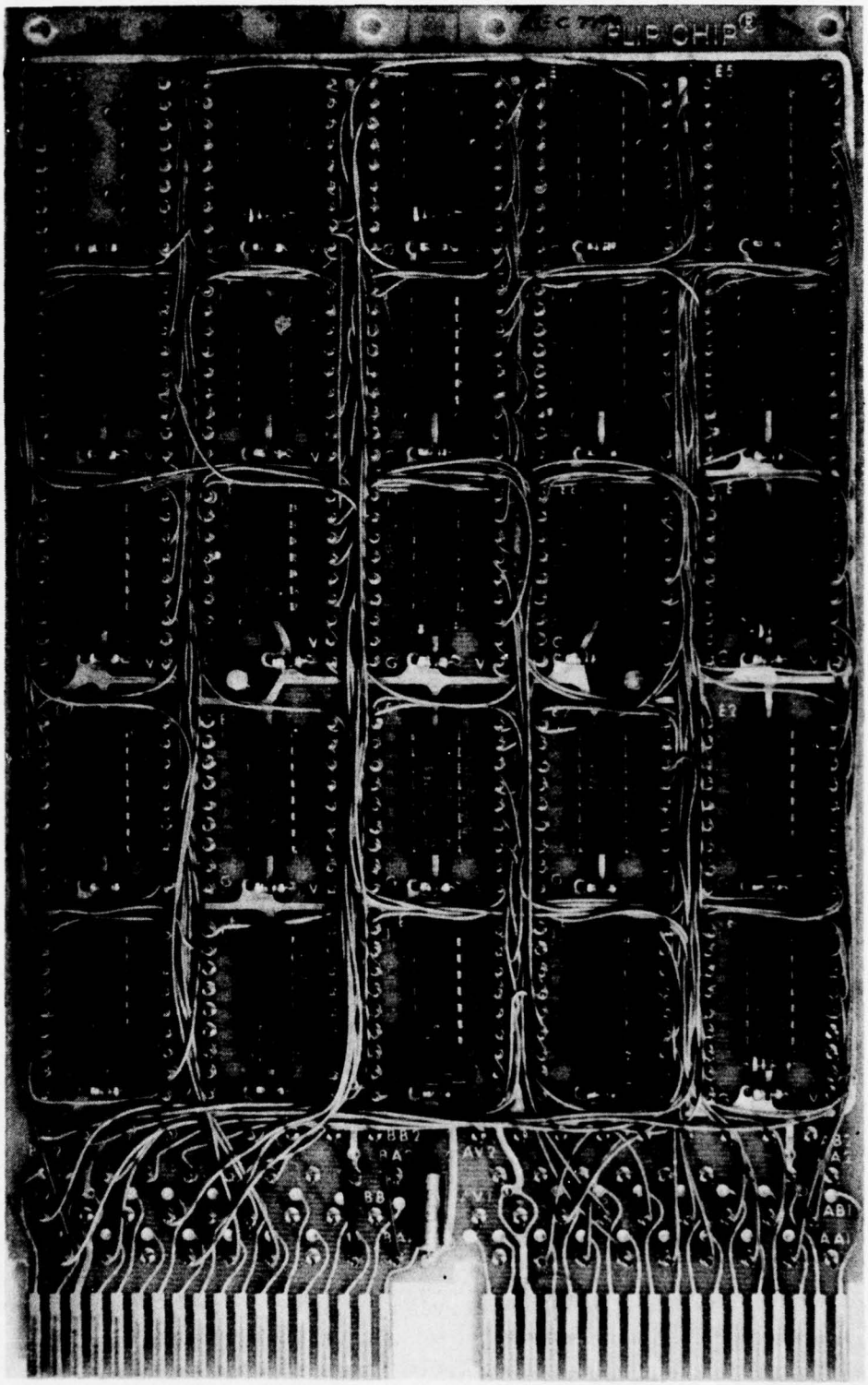


Figure 13: Record timing board.

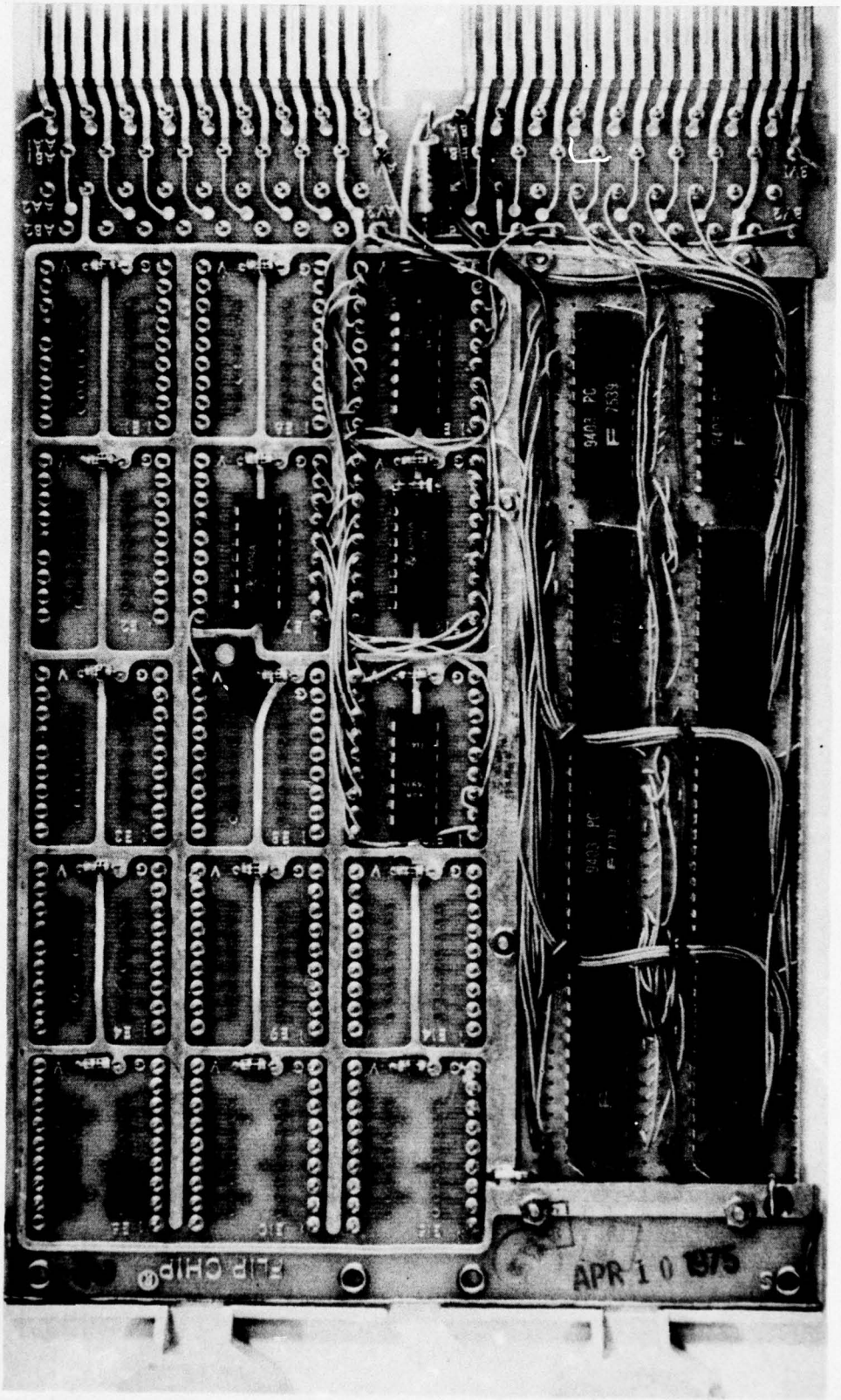


Figure 14: A record FIFO memory board.

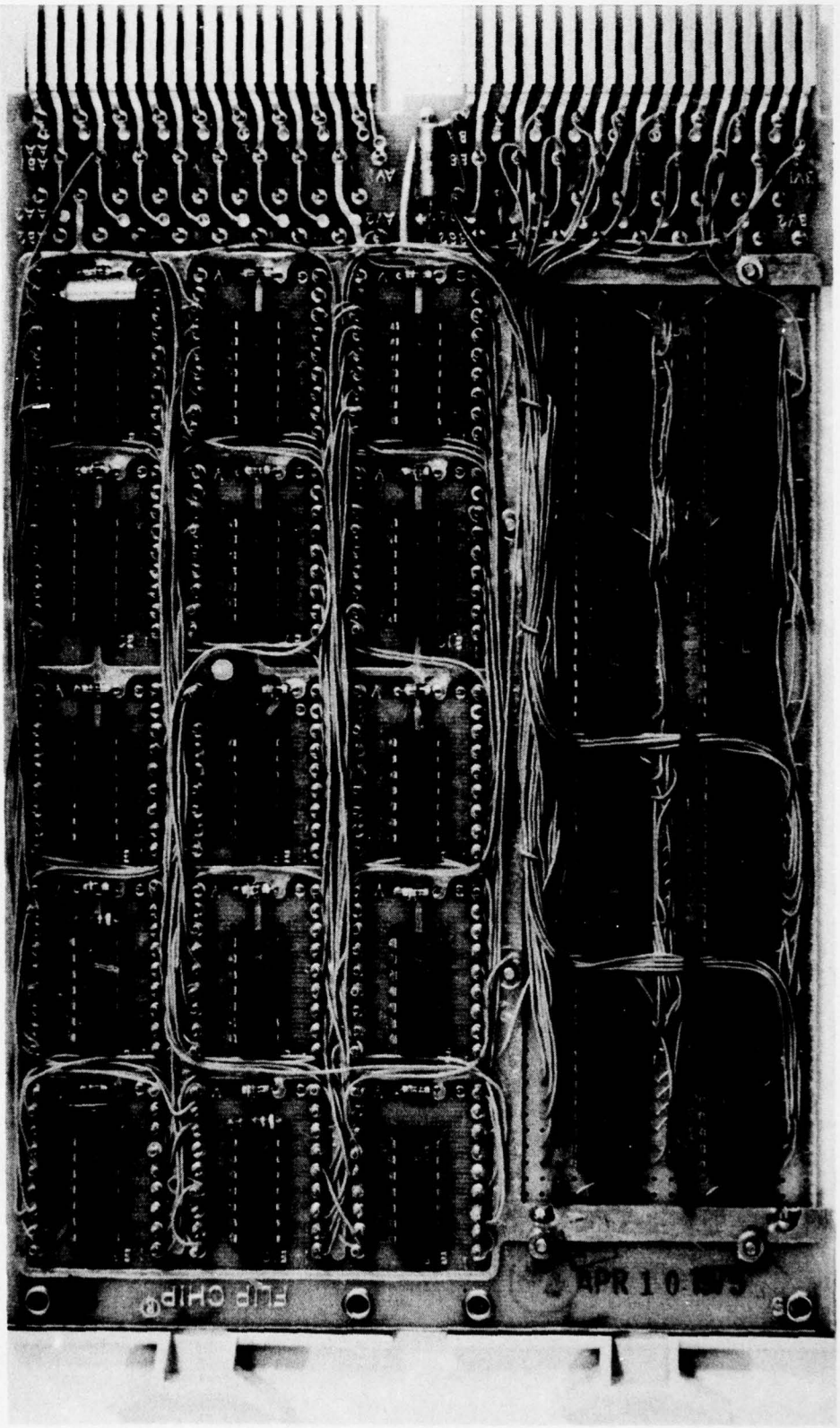


Figure 15: A reproduce FIFO memory board-component side.

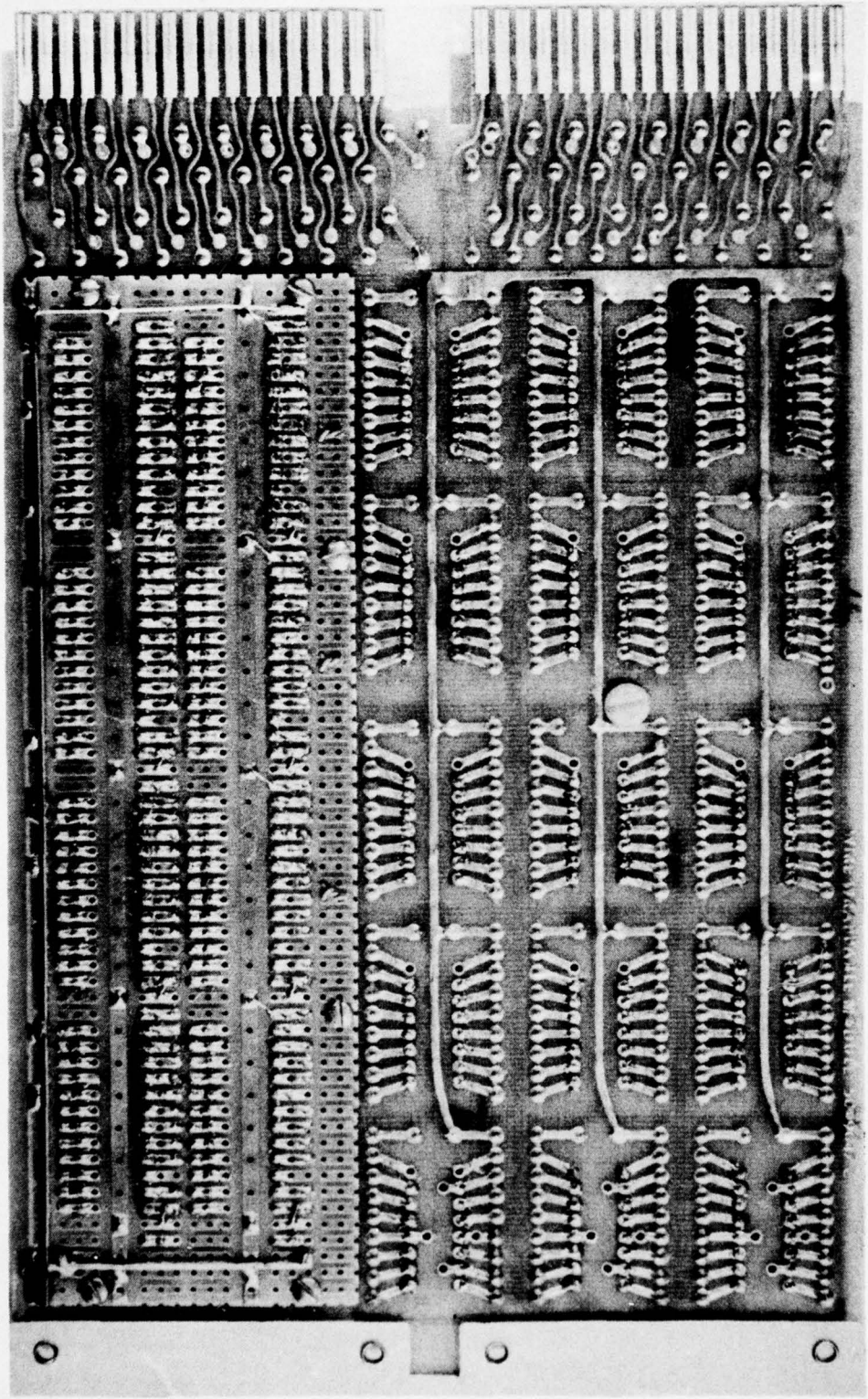


Figure 16: A reproduce FIFO memory board-printed circuit side.

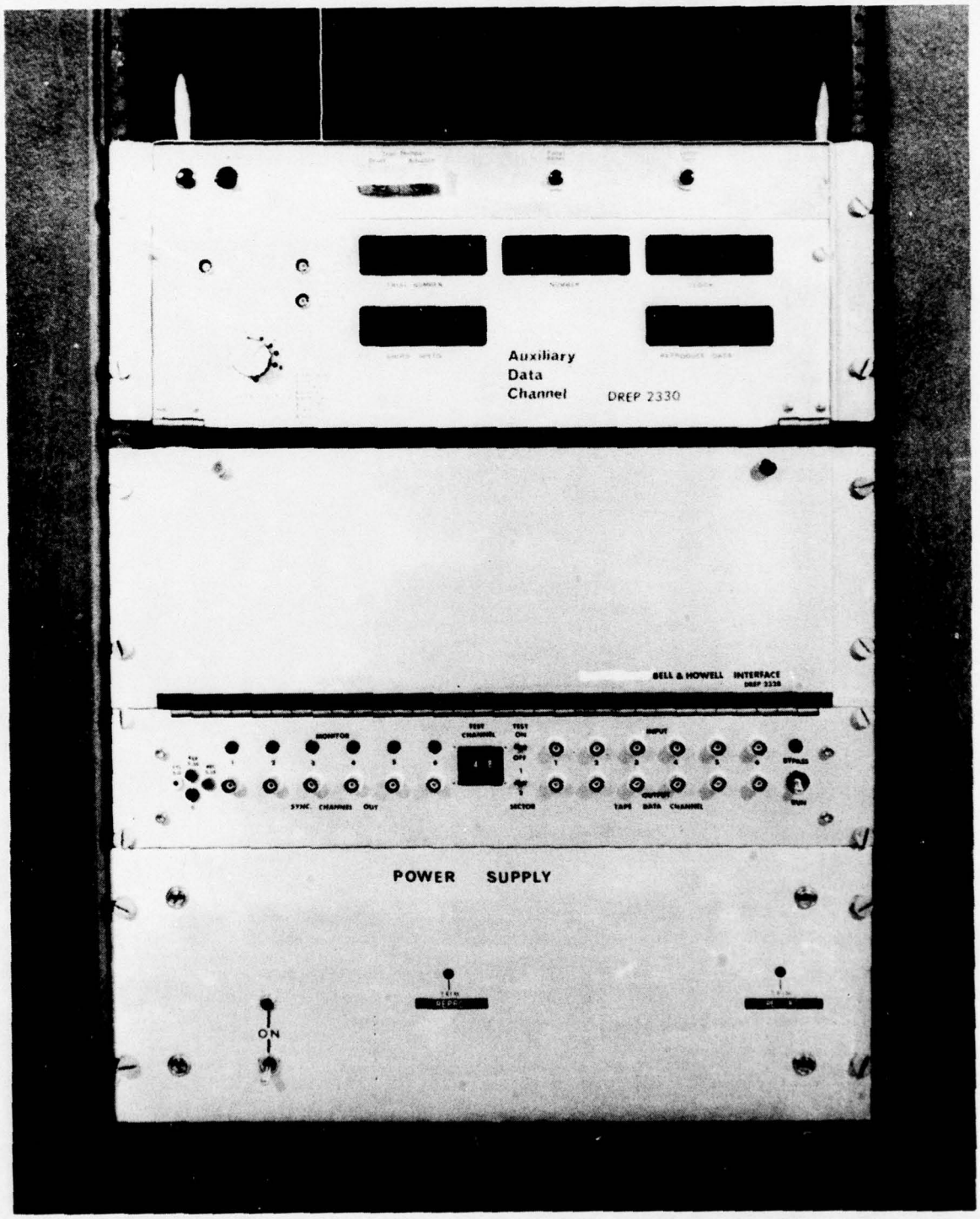


Figure 17: Front panels of the high-rate data interface system and the auxiliary data system.

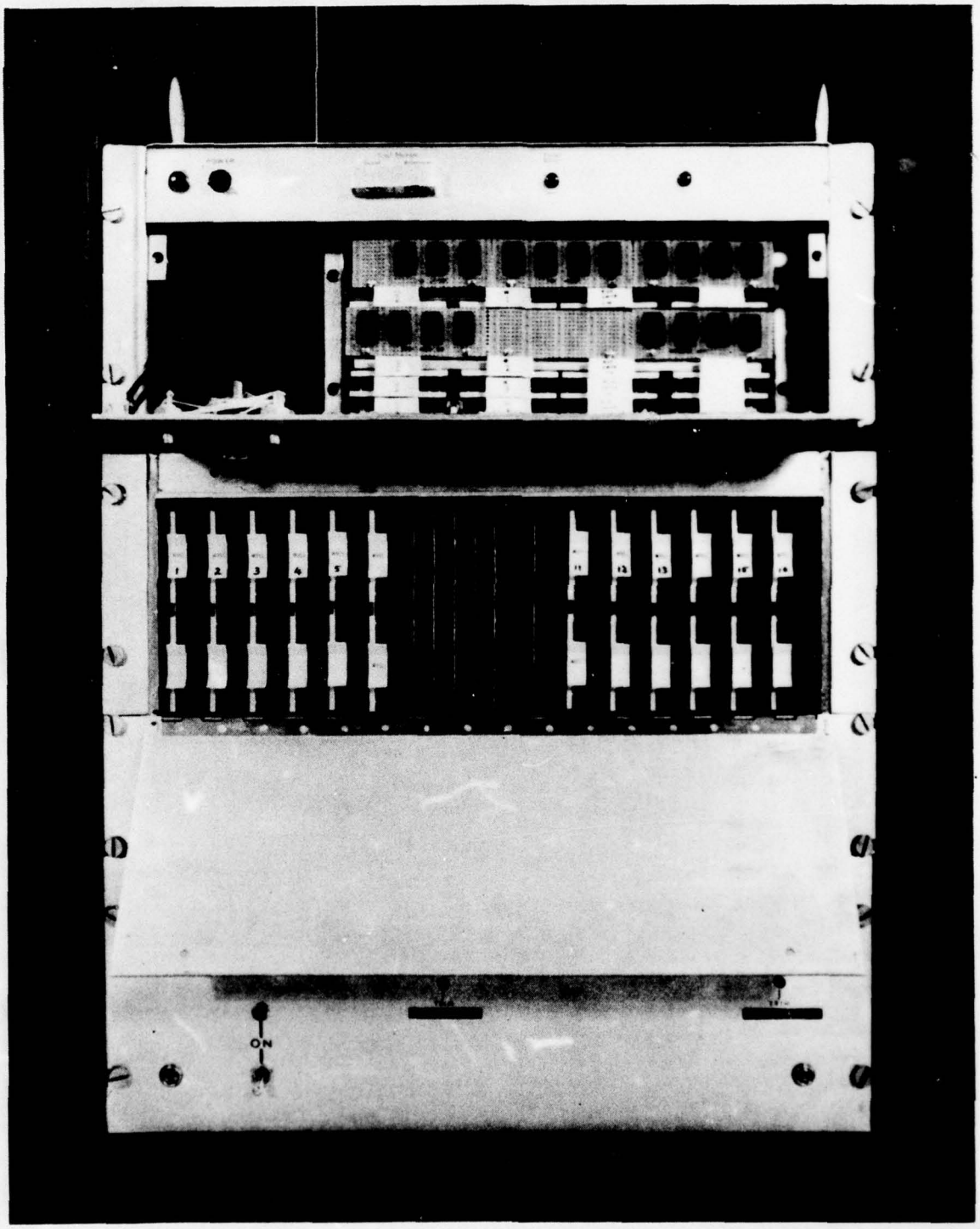


Figure 18: Front panels with access doors open

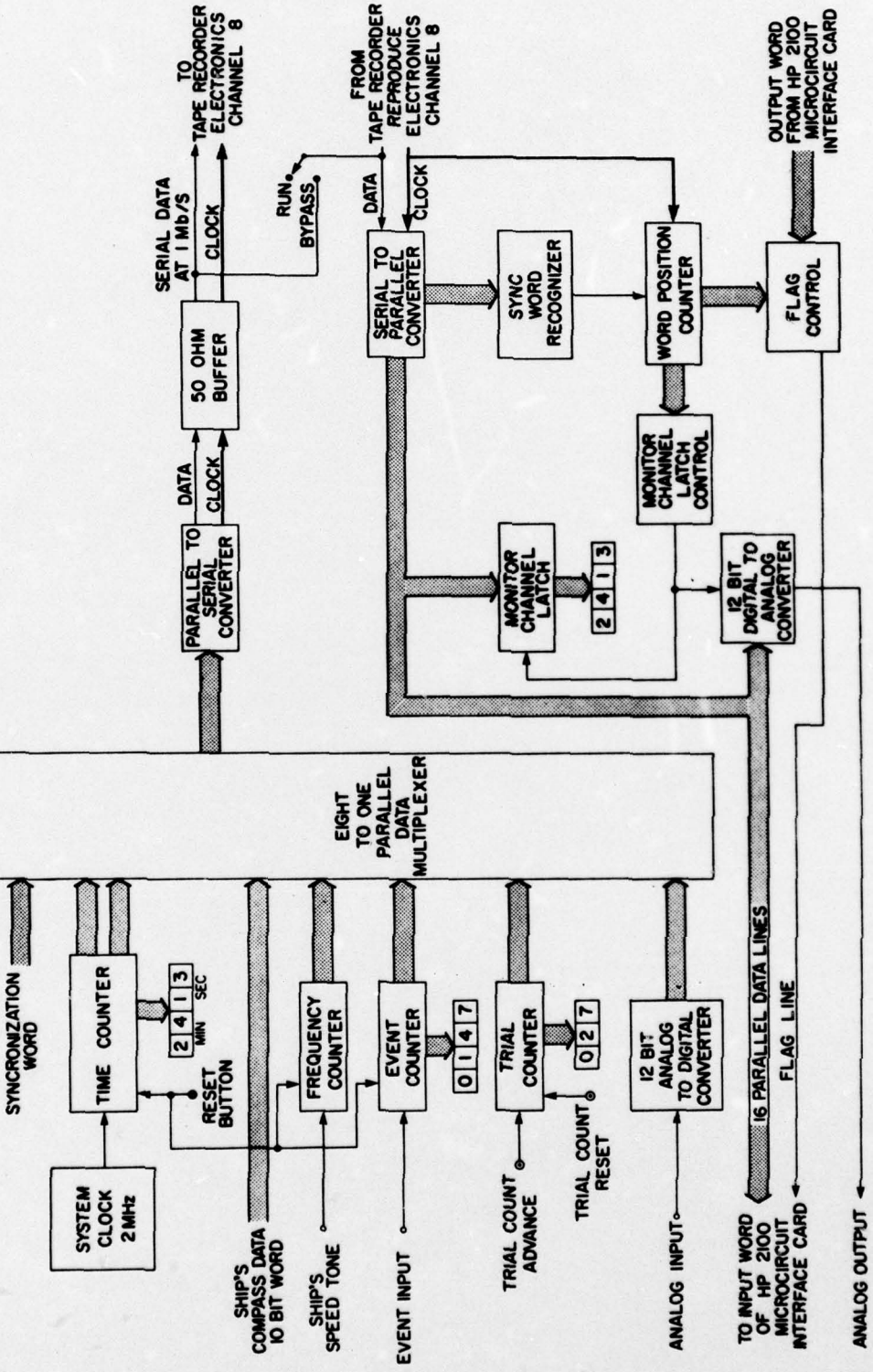


Figure 19: Auxiliary data channel system block diagram.

APPENDIX I

SPECIFICATIONS FOR THE BELL AND HOWELL VR-3700B TAPE RECORDING SYSTEM

CHARACTERISTIC	TYPICAL PERFORMANCE
System Power	115 Vac ±10% from 47-63 Hz. Approximately 1500 watts for 14 track system.
Altitude	Operating: to 12,000 ft. Storage: to 50,000 ft.
Relative Humidity	5% to 95% without condensation (tape limited).
Physical Data	
Size, Single Cabinet	72 3/4 inches high, 23 1/8 inches wide, 25 3/4 inches deep.
Weight	Approximately 800 pounds.
Paint	Cabinet, FED 595 chip 26081. Front panels, FED 595 chip 25109.
Tape Transport	
Tape Speeds	Nine, bidirectional, rotary switch selectable; 240, 120, 60, 30, 15, 7 1/2, 3 3/4, 1 7/8, and 15/16 ips.
Reels	Standard EIA to 15 inch diameter can be accommodated. Precision reels are recommended.
Tape	1/2 inch or 1 inch width standard, 1 or 1 1/2 mil mylar base. All specifications are based on Bell & Howell recommended tape.
Start Time	6 seconds maximum at 120 ips and 3 seconds at 60 ips to phase lock.
Stop Time	4 seconds maximum at 120 ips and 2 seconds maximum at 60 ips and lower speeds.
Wind/Rewind	7200 feet in less than 5 minutes.
Tape Speed Accuracy	±0.10% at all tape speeds when in tach mode. ±0.01% at all tape speeds when in tape mode.

Table 1-1. Typical Performance Characteristics

CHARACTERISTIC	TYPICAL PERFORMANCE

Flutter (Cumulative P-P)

Tape Speed (ips)	Flutter Bandwidth	% Flutter P-P
120	0.2 to 10,000 Hz	0.11
60	0.2 to 10,000 Hz	0.13
30	0.2 to 5,000 Hz	0.13
15	0.2 to 2,500 Hz	0.18
7 1/2	0.2 to 1,250 Hz	0.25
3 3/4	0.2 to 625 Hz	0.32
1 7/8	0.2 to 312 Hz	0.38
15/16	0.2 to 156 Hz	0.50

Controls

Illuminated pushbuttons for RUN FORWARD, RUN REVERSE, RECORD, FAST FORWARD, FAST REVERSE, STOP, and POWER (push-ON, push-OFF). Rotary speed selector, phase lock selector (Tape/Tach), and record test selector are front panel located. Remote control of all operating modes via connection at the transport by use of accessory Bell & Howell Remote Control Unit, or equivalent.

Dynamic Skew

Tape Speed (ips)	Microseconds (1) 0 to Peak	(2) 0 to Peak	(3) 0 to Peak
120	0.15	0.4	0.75
60	0.3	0.75	1.5
30	0.6	1.5	3.0
15	1.20	3.0	6.0
7 1/2	2.40	6.0	12.0
3 3/4	4.80	12.0	24.0
1 7/8	9.60	24.0	48.0
15/16	19.20	48.0	96.0

(1) Track to adjacent track in same head stack.
(2) Between outside tracks in same head stack - 1/2" tape.
(3) Between outside tracks in same head stack - 1" tape.

Magnetic Heads

The record and reproduce head stacks are precision mounted on plug-in subplates for easy replacement. Plug-in connector can facilitate heads with up to 42 channels.

Head and Head Stack Configuration

Per IRIG 106-71.

Table 1-1. Typical Performance Characteristics

CHARACTERISTIC	TYPICAL PERFORMANCE
Head Polarity	Per IRIG 106-71.
Head Azimuth	Record head, factory set to better than ±1 minute of arc. Reproduce head, adjustable.
Phase Lock Servo Drive	The Phase Lock Capstan Motor Control unit provides a closed loop servo operation for the dc capstan motor. This unit provides two modes of operation, tachometer and tape. When in the tachometer mode, the control servo uses the signal from the optical tachometer on the capstan drive assembly. The tachometer mode is used for initial recording. The tape control servo mode uses the prerecorded signal from the tape to establish highly accurate speeds and low time base error when reproducing tapes.
Time Base	Tape Speed (ips) / Control Reference / TBE 120 — 200 kHz — ±0.5 microsecond 60 — 100 kHz — ±0.5 microsecond 30 — 50 kHz — ±0.5 microsecond 15 — 25 kHz — ±1.0 microsecond 7 1/2 — 12.5 kHz — ±1.5 microseconds 3 3/4 — 6.25 kHz — ±3.0 microseconds 1 7/8 — 3.125 kHz — ±6.0 microseconds 15/16 — 1.5625 kHz — ±16.0 microseconds
Fail-Safe	Capstan control is automatically returned to tach mode whenever tape signal is lost or when system is placed in record mode, regardless of position of mode selector switch. Respective tach and tape lamps light only when transport is up to speed and in servo locked operation.
External Signal	External reference frequencies may be inserted for variable speed control with inclusion of optional External Reference Kit.
Data Channel	The servo control track may be used as a data channel when the optional bandpass filter card is included and provided none of the data is within one octave above or below the servo control frequency.

Table 1-1. Typical Performance Characteristics

CHARACTERISTIC	TYPICAL PERFORMANCE
Digital Electronics	
Tape Speeds	Digital electronics will accommodate any tape speed from 120 ips to 3 3/4 ips. Changing data rate is automatic with speed selection for the speeds available on the particular record and reproduce electronics installed.
Data Rates	
Enhanced NRZ	

TAPE SPEED	INPUT RATE RANGE	BIT RATE ON TAPE	RANGE OF PACKING DENSITY	BIT ERROR RATE
120 ips	0.8-3.5 Mb/s	1.0-4.0 Mb/s	8-33 kb/i	1 in 10^7
60 ips	0.44-1.76 Mb/s	0.5-2.0 Mb/s	8-33 kb/i	1 in 10^7
30 ips	0.44-0.88 Mb/s	0.5-1.0 Mb/s	16-33 kb/i	1 in 10^7
15 ips	0.22-0.44 Mb/s	0.25-0.50 Mb/s	16-33 kb/i	1 in 10^7
7 1/2 ips	110-220 kb/s	125-250 kb/s	16-33 kb/i	1 in 10^7
3 3/4 ips	88-110 kb/s	100-125 kb/s	26-33 kb/i	5 in 10^7

NOTE: Bit rates on tape are based on the use of Bell & Howell Enhanced NRZ, inserting a parity bit after every seven data bits. For non-enhanced NRZ, input data rate equals bit rate on tape.

Table 1-1. Typical Performance Characteristics

CHARACTERISTIC	TYPICAL PERFORMANCE
Data Formats	Input data, data on tape, and output data formats are available by installing the appropriate jumpers on the standard digital electronics. These formats are listed below.

INPUT DATA	DATA ON TAPE	OUTPUT DATA
NRZ - Any: L, M, S	NRZ*	NRZ - Same as Input
NRZ - Any: L, M, S	Enhanced NRZ	NRZ - Same as Input
Bi-Phase - Any: L, M, S	Bi-Phase	Bi-Phase - Same as Input
NRZ-L	Delay Modulation	Delay Modulation
Delay Modulation	Delay Modulation	Delay Modulation

*Requires customer to guarantee NRZ format contains no more than 14 consecutive ONES or 14 consecutive ZEROS.

Input Signal Levels	Input levels (both clock and data) must be standard TTL logic levels, or differential input levels compatible with type SN75107 line receivers.
Output Signal Levels	Output levels are standard TTL logic levels, or differential output from line driver. Selection is made by installation of the proper output (plug-in) components.
Phasing	NRZ data must be accompanied by a clock with transitions at midbit cell. Differential input data must be such that the clock output of the differential line receiver has transitions at midbit cell of the data output.

Table 1-1. Typical Performance Characteristics

APPENDIX II

SPECIFICATIONS FOR THE FAIRCHILD 9403

FIRST-IN FIRST-OUT BUFFER MEMORY

9403

FIRST-IN FIRST-OUT (FIFO) BUFFER MEMORY

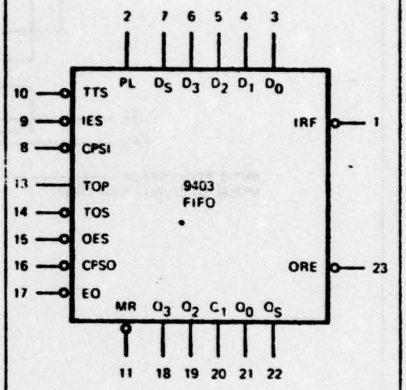
FAIRCHILD MACROLOGIC

DESCRIPTION – The 9403 is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high speed disc or tape controllers and communication buffer applications. It is organized as 16 words by four bits and may be expanded to any number of words or any number of bits (in multiples of 4). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 9403 has 3-state outputs which provide added versatility. It is a member of Fairchild's TTL MACROLOGIC family and is fully compatible with all TTL families.

- **14 MHz SERIAL OR PARALLEL DATA RATE**
- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE OUTPUTS**
- **FULLY COMPATIBLE WITH ALL TTL FAMILIES**
- **24-PIN PACKAGE**

LOGIC SYMBOL

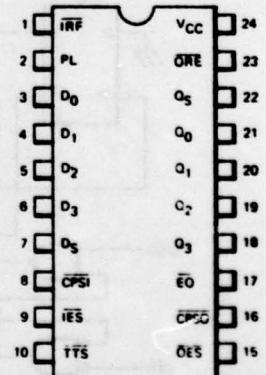


V_{CC} = Pin 24
GND = Pin 12

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
$D_0 - D_3$	Parallel Data Inputs	0.5 U.L.	0.23 U.L.
D_S	Serial Data Input	0.5 U.L.	0.23 U.L.
PL	Parallel Load Input	0.5 U.L.	0.23 U.L.
$\overline{CPSI}$	Serial Input Clock (Operates on Negative-Going Transition)	0.5 U.L.	0.23 U.L.
$\overline{IES}$	Serial Input Enable (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{TTS}$	Transfer to Stack Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{OES}$	Serial Output Enable Input (Active LOW)	0.5 U.L.	0.25 U.L.
$\overline{TOS}$	Transfer Out Serial Input (Active LOW)	0.5 U.L.	0.23 U.L.
TOP	Transfer Out Parallel Input	0.5 U.L.	0.23 U.L.
$\overline{MR}$	Master Reset (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{CPSO}$	Serial Output Clock Input (Operates on Negative-Going Transition)	0.5 U.L.	0.23 U.L.
$Q_0 - Q_3$	Parallel Data Outputs (Note b)	130 U.L.	10 U.L.
Q_S	Serial Data Output (Note b)	10 U.L.	10 U.L.
$\overline{IRF}$	Input Register Full Output (Active LOW) (Note b)	10 U.L.	5 U.L.
$\overline{ORE}$	Output Register Empty Output (Active LOW) (Note b)	10 U.L.	5 U.L.

NOTES:
a. 1 unit load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. Output fan-out with $V_{OL} \leq 0.5$ V

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

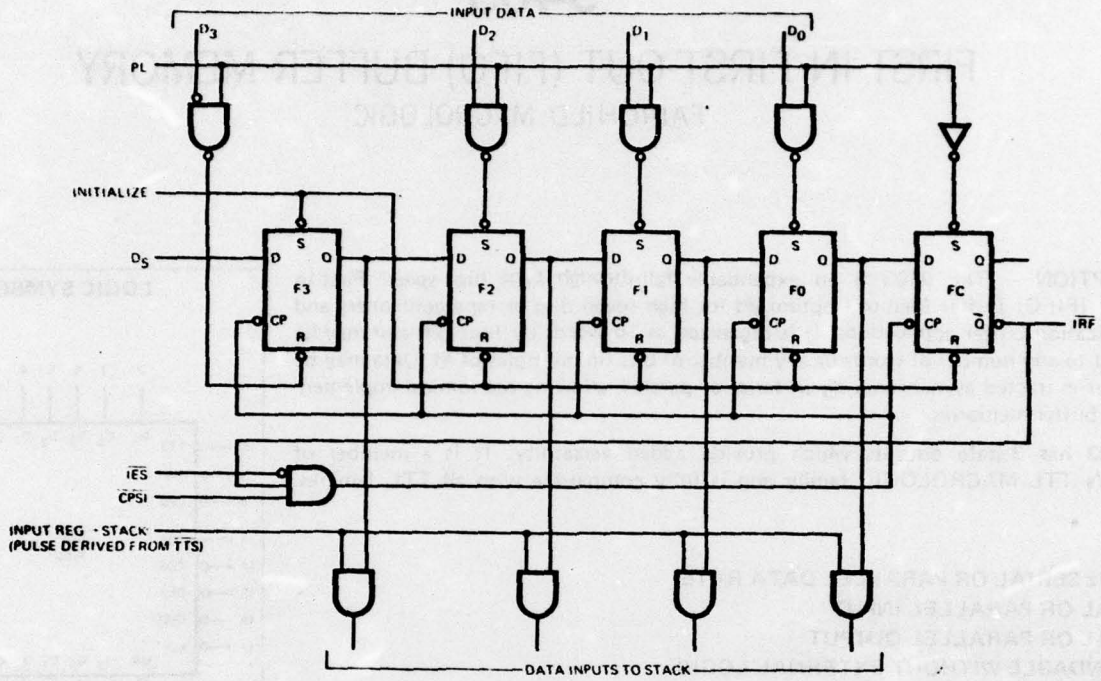


Fig. 1
CONCEPTUAL INPUT SECTION

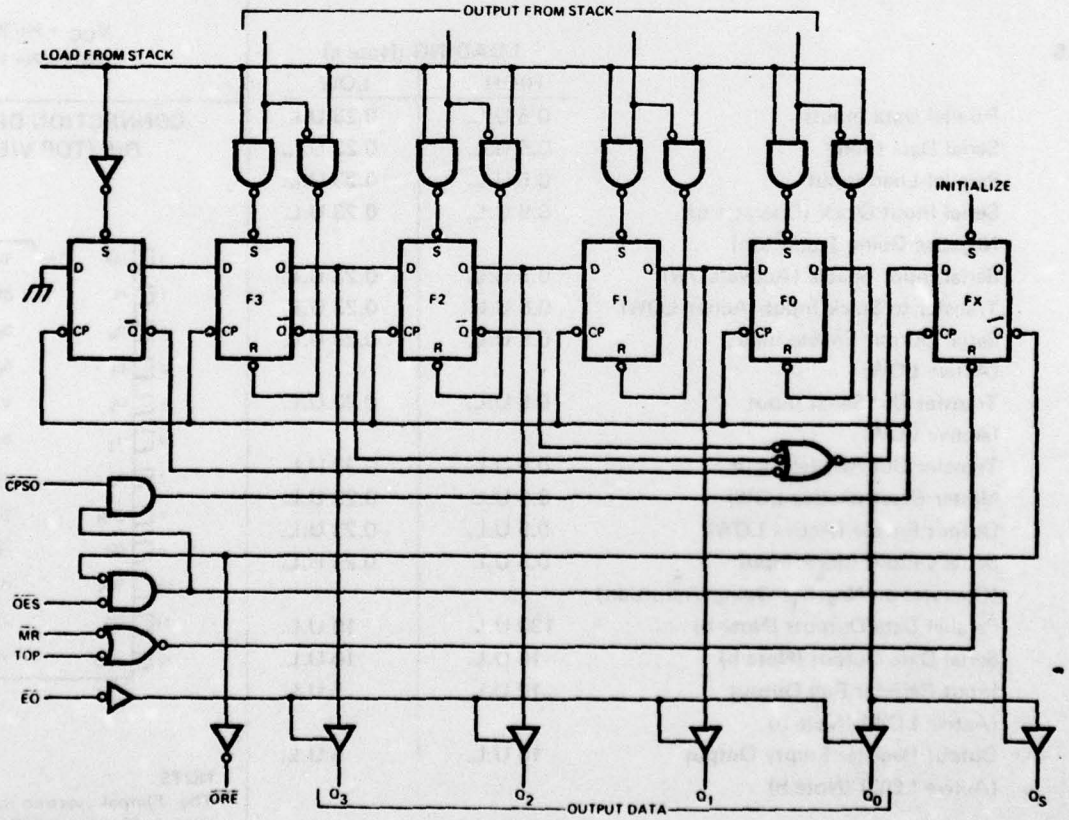
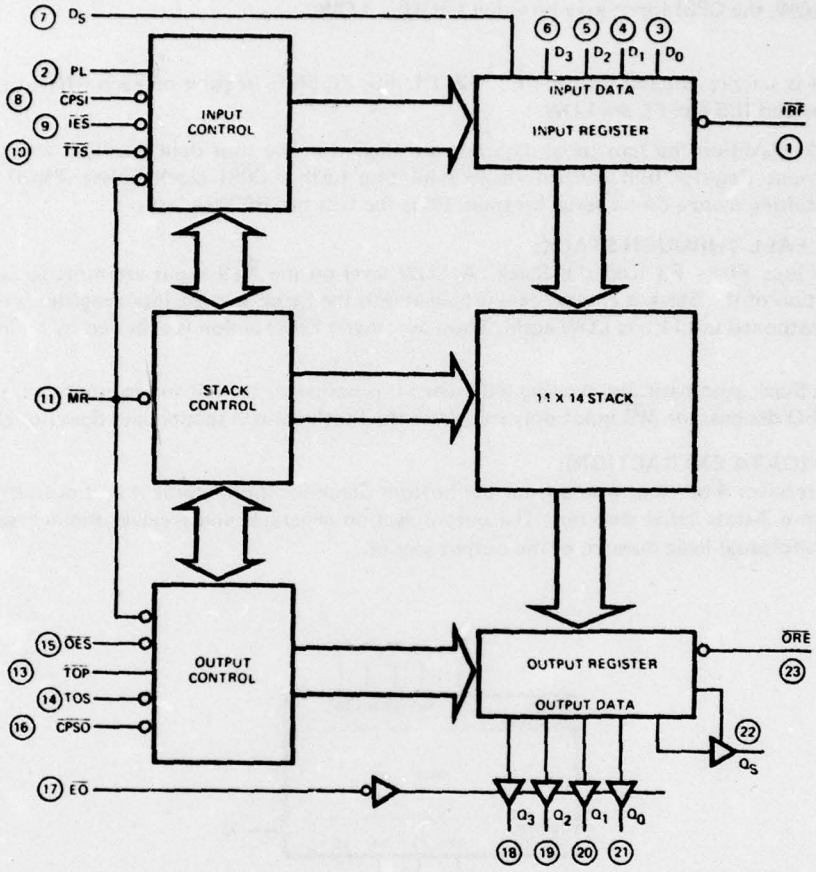


Fig. 2
CONCEPTUAL OUTPUT SECTION

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – As shown in the Block Diagram the 9403 consists of three parts:

1. An Input Register with Parallel and Serial Data Inputs as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit wide, 14-word deep Fall-Through Stack with self-contained control logic.
3. An Output Register with Parallel and Serial Data Outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below:

INPUT REGISTER (DATA ENTRY):

The Input Register can receive data in either bit-serial or in 4-bit parallel form, store it until it is sent to the Fall-Through Stack and generate and accept the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F3 Flip-Flop and resetting the other flip-flops. The $\overline{Q}$ Output of the last Flip-Flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

PARALLEL ENTRY:
A HIGH level on the PL Input loads the $D_0 - D_3$ Data Inputs into the F0 – F3 Flip-Flops and sets the FC Flip-Flop, which forces $\overline{IRF}$ LOW, indicating "Input Register Full". The D Inputs must be stable while PL is HIGH. During parallel entry, the $\overline{IES}$ Input should be LOW; the $\overline{CPSI}$ Input may be either HIGH or LOW.

SERIAL ENTRY:
Data on the DS Input is serially entered into the F3, F2, F1, F0, FC Shift Register on each HIGH-to-LOW transition of the $\overline{CPSI}$ Clock Input, provided $\overline{IES}$ and PL are LOW.

After the fourth clock transition the four serial data bits are aligned in the four data flip-flops and the FC Flip-Flop is set, forcing $\overline{IRF}$ LOW (Input Register full) and internally inhibiting further $\overline{CPSI}$ clock pulses. Figure 3 illustrates the final positions in a 9403 resulting from a 64-bit serial bit train. B0 is the first bit, B63 the last bit.

TRANSFER TO THE FALL-THROUGH STACK:
The outputs of Flip-Flops F0 – F3 feed the Stack. A LOW level on the $\overline{TTS}$ Input attempts to initiate a "fall-through" action. If the top location of the Stack is empty, data is loaded into the Stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

Data falls through the Stack automatically, pausing only when it is necessary to wait for an empty next location. In the 9403, as in most modern FIFO designs, the $\overline{MR}$ input only initializes the Stack control section and does not clear the data.

OUTPUT REGISTER (DATA EXTRACTION):
The Output Register receives 4-bit data words from the bottom Stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. Figure 2 is a conceptual logic diagram of the output section.

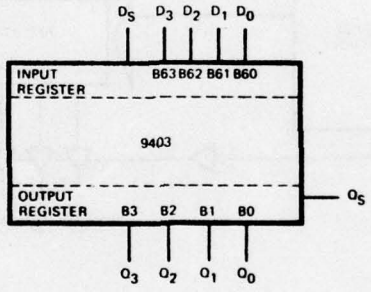


Fig. 3
FINAL POSITIONS IN A 9403 RESULTING FROM A 64-BIT SERIAL TRAIN

PARALLEL DATA EXTRACTION:
When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) Output is LOW. After data has been entered into the FIFO and has fallen through to the bottom Stack location, it is transferred into the output register, provided the "Transfer Out Parallel" (TOP) Input is HIGH, and the $\overline{OES}$ Input is LOW. As a result of the data transfer $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{ORE}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next LOW-to-HIGH transition of TOP transfers the next word (if available) into the output register as explained above. During parallel data extraction, $\overline{TOS}$, $\overline{CPSO}$, and $\overline{OES}$ should be LOW.

SERIAL DATA EXTRACTION:
When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom Stack location, it is transferred into the output shift register provided the "Transfer Out Serial" ($\overline{TOS}$) is LOW. TOP must be HIGH, and $\overline{OES}$ and $\overline{CPSO}$ must be LOW. As a result of the data transfer $\overline{ORE}$ goes HIGH indicating valid data in the shift register. The 3-state serial Data Output O_S is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. The fourth transition empties the shift register, forces $\overline{ORE}$ LOW and disables the serial output O_S. For serial operation the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the Stack as soon as the previous one has been shifted out.

EXPANSION:

Vertical Expansion – The 9403 may be vertically expanded to store more words without external parts. The interconnections necessary to form a 46-word by 4-bit FIFO are shown in Figure 4. Using the same technique, any FIFO of 15n + 1 words by four bits can be constructed. Note that expansion does ot sacrifice any of the FIFO's flexibility for serial/parallel input and output.

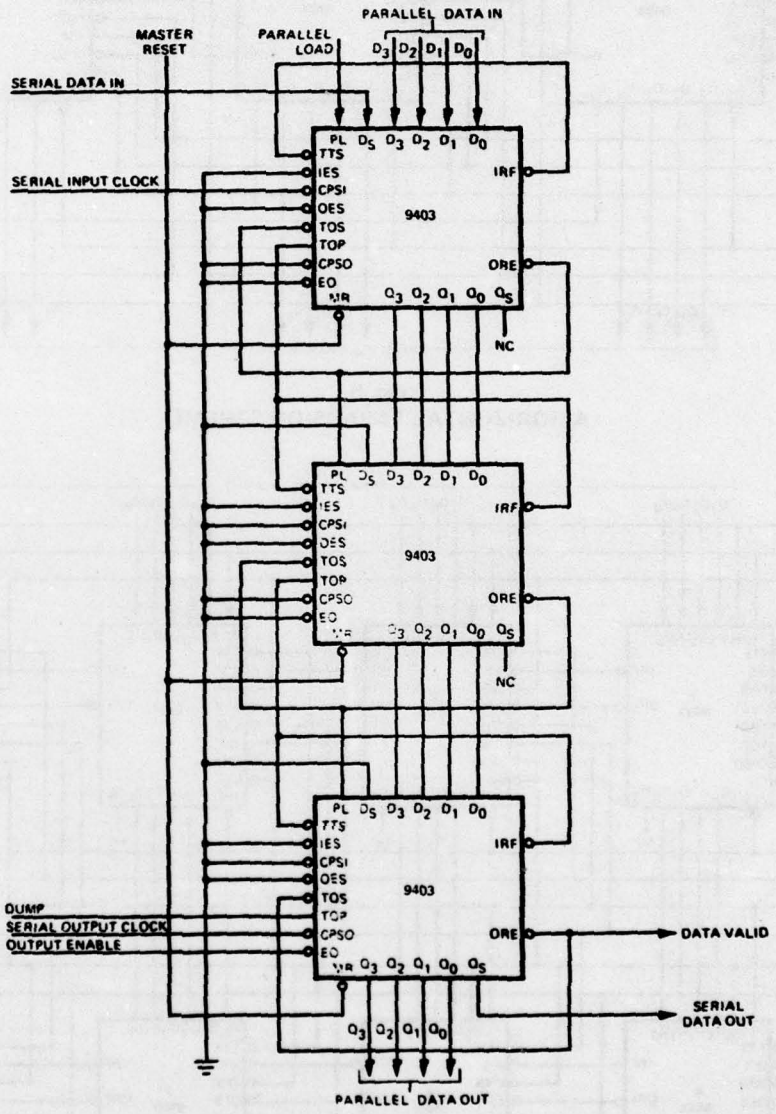


Fig. 4
A VERTICAL EXPANSION SCHEME

Horizontal Expansion – The 9403 may also be horizontally expanded to store long words (in multiples of four bits) without external logic. The interconnections necessary to form a 16-word by 12-bit FIFO are shown in Figure 5. Using the same technique, any FIFO of 16 words by 4 X n bits can be constructed. When expanding in the horizontal direction, it is usual to connect the $\overline{IRF}$ and $\overline{ORE}$ outputs of the right most device (most significant device) to the $\overline{TTS}$ and $\overline{TOS}$ inputs respectively of all devices to the left (less significant devices) to guarantee that no operation is initiated before all devices are ready.

As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the FIFO's flexibility for serial/parallel input and output.

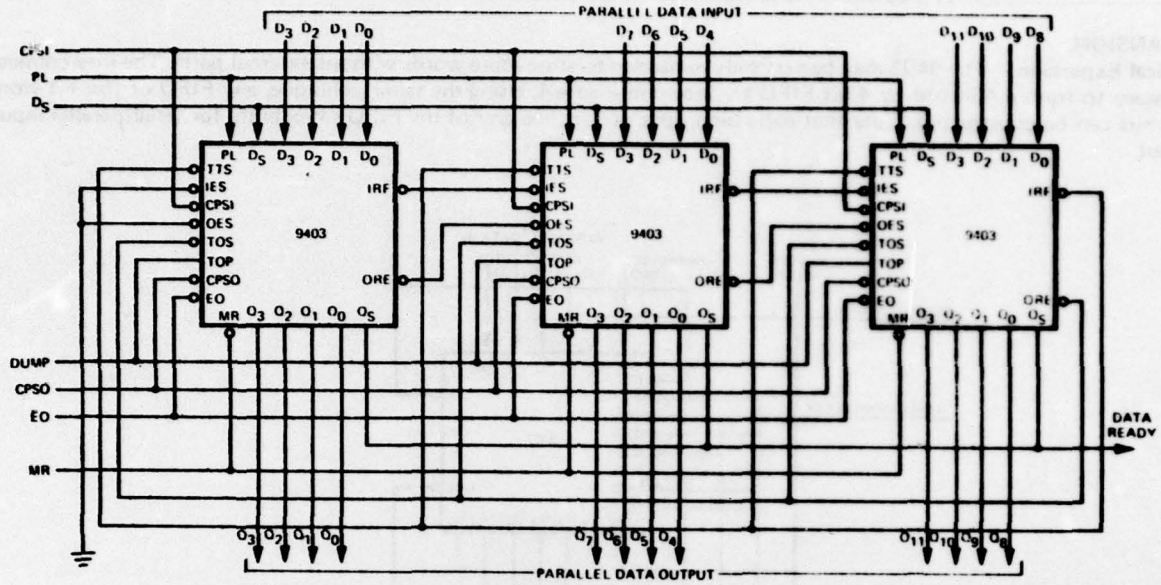


Fig. 5
A HORIZONTAL EXPANSION SCHEME

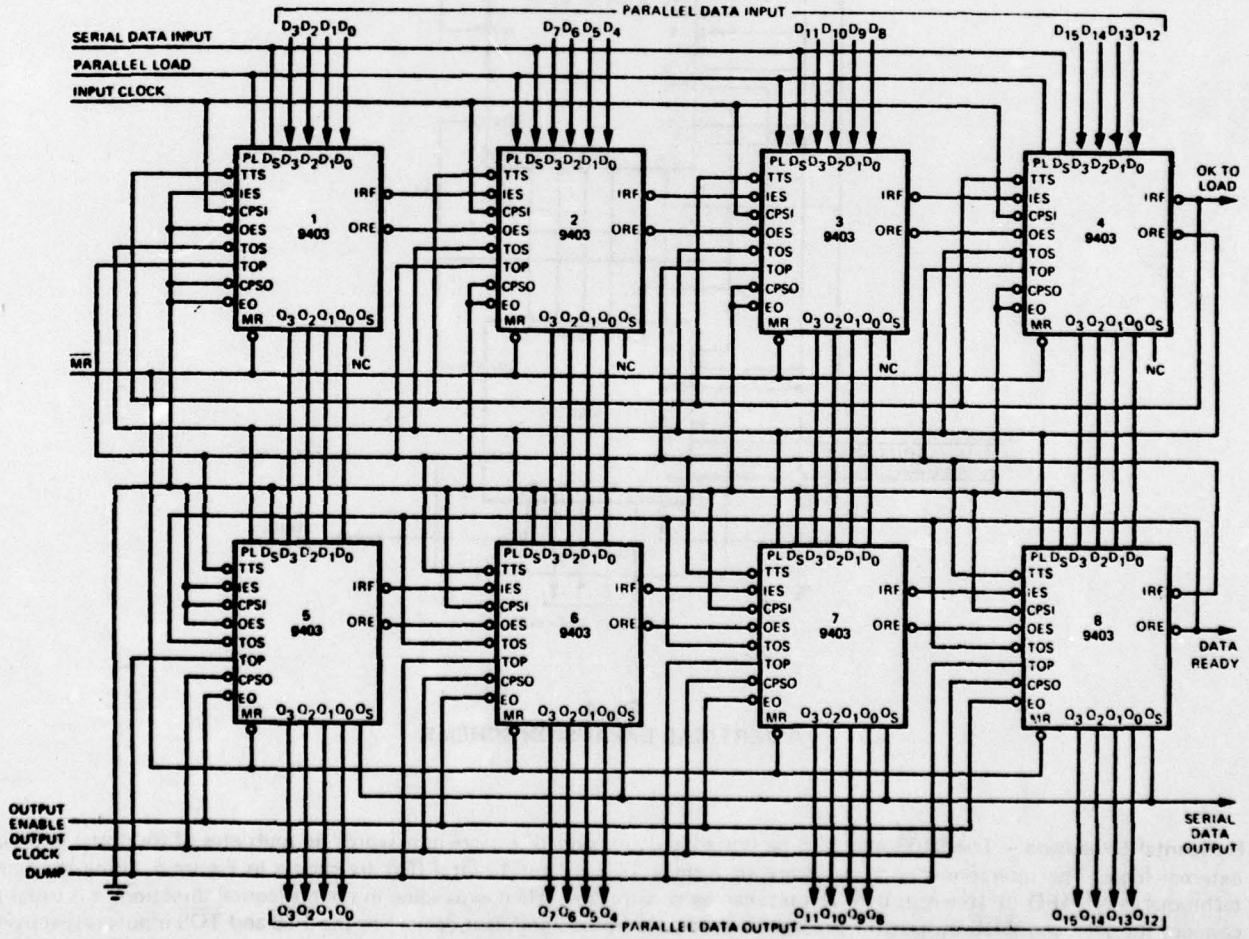


Fig. 6
A 31 X 16 FIFO ARRAY